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(54) DIGITAL SIGNAL DELIVERING SYSTEM, DIGITAL AUDIO SIGNAL PROCESSING CIRCUIT AND SIGNAL CONVERTING CIRCUIT

(57)Abstract:

PURPOSE: To provide a digital signal delivering system to realize the selling of information, etc., having the commercial value in the condition of the mode of a digital signal, an audio processing circuit suitable for it, a signal processing circuit, etc.

CONSTITUTION: In the delivery of a digital signal, a digital signal supply source and a player are directly connected, the specified information is received and stored, and the information stored by the player itself is reproduced. A terminal device 100 plays the role of an information server and is arranged at the station store, etc. The terminal device 100 is constituted of an input part 102, a storage part 103 and an output part 104, each circuit block is connected by a VME bus 105, and a digital signal and respective types of control signals are given and received. A memory card 101 (a player) with a reproduction function illustrated by dotted lines is connected and a special digital signal as merchandise is delivered as it is.

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2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The digital signal delivery system which is connected with the above-mentioned digital signal supply source in a digital signal supply source and delivery of a digital signal, and is characterized by coming to have the memory card with a regenerative function which reproduces the digital signal which memorized to the reception store circuit and was independently memorized with the specified digital signal.

[Claim 2] The digital signal delivery system of claim 1 characterized by delivering a digital signal between the above-mentioned digital signal supply source and the above-mentioned memory card with a regenerative function at a rate quicker than the signal processed at least in the above-mentioned digital signal delivery system.

[Claim 3] It connects with the above-mentioned digital signal supply source in the above-mentioned digital signal supply source and delivery of a digital signal. And it sets to the digital signal delivery system equipped with the memory card with a regenerative function which reproduces the digital signal which memorized to the reception store circuit and was independently memorized with the specified digital signal. While carrying out the reception storage of the digital signal through a communication line or a suitable storage if needed from the supply origin of a digital signal, and this supply origin, the above-mentioned digital signal supply source The digital signal delivery system of claim 1 characterized by being what consists of a terminal unit which is connected with the above-mentioned memory card with a regenerative function through a connector, and delivers the specified digital signal.

[Claim 4] It compares with the storage capacity of the store circuit on a memory card with a regenerative function, and the storage capacity of the above-mentioned terminal unit is the same or a digital signal delivery system of claim 3 characterized by being the storage capacity beyond it.

[Claim 5] The above-mentioned terminal unit is the digital signal delivery system of claim 3 characterized by being the thing which makes the buffer memory constituted by the semiconductor memory in which rapid access is possible memorize the digital signal which delivers between memory cards with a regenerative function, and is updated with a digital signal or the passage of time with many amounts, using magnetic disk memory equipment with comparatively big memory capacity as a backup memory.

[Claim 6] The above-mentioned terminal unit is the digital signal delivery system of claim 3 characterized by being what also performs management of the storage area to

the store circuit in the memory card with a regenerative function in the condition of having connected besides having microcomputer ability, and delivering and receiving a digital signal with a supplying agency through management and the communication line of the above-mentioned magnetic disk memory or buffer memory, claim 4, or claim 5.

[Claim 7] The above-mentioned terminal unit is the digital signal delivery system of claim 3** characterized by being a thing with the function to which a part of specified digital signal is made to restrict, reproduce and output to fixed time amount.

[Claim 8] It connects with the above-mentioned digital signal supply source in a digital signal supply source and delivery of a digital signal. And it sets to the digital signal delivery system equipped with the memory card with a regenerative function which reproduces the digital signal which memorized to the reception store circuit and was independently memorized with the specified digital signal. The above-mentioned memory card with a regenerative function is a memory card with a regenerative function characterized by being that to which charge actuation is also performed to the above-mentioned rechargeable battery according to the power source by the side of a terminal unit when a rechargeable battery is built in and it connects with the above-mentioned terminal unit.

[Claim 9] The above-mentioned memory card with a regenerative function is a memory card with a regenerative function of claim 8 characterized by being a thing equipped with the playback output circuit which makes the digital sound signal by which reading appearance was carried out change and output to an analog sound signal from a store circuit.

[Claim 10] The above-mentioned memory card with a regenerative function is a memory card with a regenerative function of claim 9 characterized by being separation or the thing by which desorption is carried out at the storage of the shape of a thin card.

[Claim 11] The above-mentioned memory card with a regenerative function is a memory card with a regenerative function of claim 9 characterized by being that by which automatic assignment of the playback conditions is carried out according to the content of the ID code with an ID code.

[Claim 12] The above-mentioned playback conditions are the memory card with a regenerative function of claim 11 characterized by being a thing containing at least one of the resolution and the sampling frequencies which consist of a stereo / monophonic playback, 8 bits, and 16 bits.

[Claim 13] It connects with the above-mentioned digital signal supply source in a digital signal supply source and delivery of a digital signal. And it sets to the digital signal delivery system equipped with the memory card with a regenerative function which reproduces the digital signal which memorized to the reception store circuit and was independently memorized with the specified digital signal. The above-mentioned memory card with a regenerative function is a memory card with a regenerative

function characterized by having the store circuit and the connector for carrier delivery of the signal from the outside which carry out storage control of the above-mentioned digital signal, and the control unit which controls playback.

[Claim 14] The memory card with a regenerative function of claim 13 which is the connector which applies to the above-mentioned connector for carrier delivery at JEIDA specification or JEIDA specification.

[Claim 15] It connects with the above-mentioned digital signal supply source in a digital signal supply source and delivery of a digital signal. And it sets to the digital signal delivery system equipped with the memory card with a regenerative function which reproduces the digital signal which memorized to the reception store circuit and was independently memorized with the specified digital signal. The above-mentioned store circuit reverses at least 1-bit digital signal of the input of the above-mentioned store circuit, and/or the output section according to the coincidence detecting signal of a password or a password. Or the store circuit characterized by being a thing with a security function which changes for other bits and does not reproduce a right digital signal to a user.

[Claim 16] The above-mentioned store circuit is a store circuit of claim 15 characterized by being a thing with a security function which is made to reverse at least 1-bit digital signal of the address input section of a store circuit according to the coincidence detecting signal of a password or a password, or changes for other bits, and does not reproduce a right digital signal to a user.

[Claim 17] The above-mentioned store circuit is a store circuit of claim 15 which makes an invalid at least 1-bit digital signal of the output section of the above-mentioned store circuit according to the coincidence detecting signal of a password or a password, or is characterized by being a thing with the security function which changes for other bits and prevented from reading a right digital signal outside from the above-mentioned memory card with a regenerative function.

[Claim 18] The above-mentioned store circuit is a store circuit of claim 15 which makes an invalid at least 1-bit digital signal of the address input section of the above-mentioned store circuit according to the coincidence detecting signal of a password or a password, or is characterized by being a thing with the security function which changes for other bits and prevented from reading a right digital signal outside from the above-mentioned memory card with a regenerative function.

[Claim 19] The store circuit of claim 15 characterized by enabling it to choose the information on arbitration from the information which divided the above-mentioned store circuit into the storage capacity of arbitration, and memorized the information from which plurality differed, and the user memorized at the time of playback.

[Claim 20] The above-mentioned store circuit is a store circuit of claim 15 characterized by coming to have the storage region or table-of-contents store circuit which memorizes table-of-contents information including the storing address

corresponding to two or more digital signals, and the data area or data store circuit accessed by the above-mentioned storing address.

[Claim 21] The above-mentioned control unit is the memory card with a regenerative function of claim 13 characterized by being that to which assignment of a mode of operation which consists of two or more kinds is performed by the ON time amount or the count of ON of one key switch.

[Claim 22] It connects with the above-mentioned digital signal supply source in a digital signal supply source and delivery of a digital signal. And it sets to the digital signal delivery system which comes to have the memory card with a regenerative function which reproduces the digital signal which memorized to the reception store circuit and was independently memorized with the specified digital signal. The digital signal delivery system characterized by the trowel which established a means to compress or elongate amount of information to the original amount of information of the above-mentioned digital signal, and a noise rejection means to remove a noise.

[Claim 23] The above-mentioned noise rejection means is the digital signal delivery system of claim 22 characterized by consisting of the means which transposes compulsorily the digital signal inputted into a digital to analog circuit in a means to detect the silent period of the digitized sound signal, and its silent period to the signal corresponding to 0 alternating current level.

[Claim 24] The above-mentioned noise rejection means is a digital signal delivery system of claim 22 by which the above-mentioned silent period is characterized by being in a predetermined period silent condition based on the comparison means and the above-mentioned comparison result which compare the predetermined level and the predetermined digital signal of positive/negative amphipathy consider that is silent respectively at the time less than of predetermined level.

[Claim 25] The digital signal delivery system of claim 22 characterized by performing ****** playback with a means to detect the silent period of the sound signal by which the above-mentioned means which carries out expanding was digitized, and to expand the silent period.

[Claim 26] The means to which the above-mentioned silent period is made to expand is the digital signal delivery system of claim 25 characterized by being what performed by **(ing) substantially renewal actuation of the address of the memory circuit in which the digital signal was stored compared with normal operation.

[Claim 27] The digital signal delivery system of claim 22 characterized by reproducing by detecting the silent period of the sound signal by which the above-mentioned means which carries out compression was digitized, shortening the silent period, and already hearing it.

[Claim 28] A means to shorten the above-mentioned silent period is the digital signal delivery system of claim 27 characterized by being what performed by making quick renewal actuation of the address of the memory circuit in which the digital signal was

stored compared with normal operation.

[Claim 29] The digital signal delivery system of claim 22 characterized by to consist of the means to which a subtraction result makes output with the above-mentioned data by which compression is carried out when small, a means output the maximum of a means ask for difference with the data into which the above-mentioned means which carries out compression was inputted as the sampling data in front of [of the above-mentioned digital signal] one, and the data compressed when larger than the maximum of the sign into which the result is compressed, and.

[Claim 30] For the data of the above-mentioned digital signal, the above-mentioned means which carries out expanding is the digital signal delivery system of claim 22 by which it is characterized by being that by which the data of a basis develop from being added with the sampling data in front of one.

[Claim 31] While a data compression is performed by transposing the silent period of a digital signal to silent code information and a silent hour entry If silent code information is detected at the time of normal operation, while stopping the renewal actuation of the address of a memory circuit over the time amount corresponding to a silent hour entry, the signal corresponding to 0 alternating current level is made to output instead of it. If silent code information is detected at the time of ****** playback actuation, while stopping the renewal actuation of the address of a memory circuit over the time amount to which it was made to expand to a silent hour entry, the signal corresponding to 0 alternating current level is made to output instead of it. The digital-signal-processing circuit characterized by being the thing to which already hear it, the above-mentioned silent code information and a silent hour entry are substantially disregarded at the time of actuation, and a digital signal is made to output.

[Claim 32] The above-mentioned silent code information is the digital-signal-processing circuit of claim 31 characterized by being what constituted by the combination of at least two continuous digital signals corresponding to almost forward maximum and almost negative maximum.

[Claim 33] The digital-signal-processing circuit of claim 31 where the silent period which set up the maximum silent time amount and was expanded with ****** actuation is characterized by preparing the function to restrict the above-mentioned maximum silent time amount so that there may be no **.

[Claim 34] the store circuit which receives a digital input signal, and counting corresponding to [receive a conventional-time pulse and] the maximum of a digital input signal -- with the counter circuit which operates The comparator which compares the output signal of the above-mentioned store circuit with the output signal of a counter circuit, the repeat of the above-mentioned counter circuit -- counting, while instructing the incorporation of the input digital signal to a store circuit to be the repeat counter which carries out counting of the actuation in response to a

strobe signal counting of the above-mentioned counter circuit -- the signal transformation circuit characterized by acquiring the Pulse-Density-Modulation signal corresponding to a digital input signal from the output of the above-mentioned comparator including the control circuit which is made to start actuation and sends out a conversion terminate signal with the output signal from the above-mentioned repeat counter.

[Claim 35] The signal transformation circuit characterized by acquiring the Pulse-Density-Modulation signal corresponding to the above-mentioned digital input signal including the down counter circuit which receives the digital input signal supplied by the fixed period corresponding to the maximum of a digital signal, and carries out counting of the conventional-time pulse, and the digital circuit which forms the pulse corresponding to the period of the above-mentioned down counter circuit of operation.

[Claim 36] counting corresponding to [in response to the above-mentioned conventional-time pulse] a digital input signal in the fixed period corresponding to the maximum of the above-mentioned digital signal -- the signal transformation circuit of claim 35 characterized by being what formed of the rise counter circuit which operates.

[Claim 37] The above-mentioned Pulse-Density-Modulation signal is the signal transformation circuit of claim 34 characterized by being what is inputted into the low pass filter which consists of resistance and a capacitor, and changed into an analog signal.

[Claim 38] the digital to analog circuit excluding [on a digital sound signal regenerative circuit equipped with the regenerative circuit which memorizes a digital sound signal to a store circuit, carries out reading appearance of the digital sound signal from a store circuit independently, changes the digital sound signal into an analog sound signal in a digital to analog circuit, and is amplified and outputted via a low pass filter in an amplifying circuit, and] the above-mentioned store circuit, a low pass filter, and an amplifying circuit -- and the one chip integrated circuit characterized by to dedicate to a control circuit and the 1 chip integrated circuit which consists of the interface section.

[Claim 39] The one chip integrated circuit of claim 38 characterized by having the function which can extend a store circuit control function in the exterior of 1 chip integrated circuit easily in the above-mentioned digital sound signal regenerative circuit when memory capacity becomes larger than controllable memory capacity.

[Claim 40] The one chip integrated circuit of claim 38 characterized by to have the signal terminal with which the interface section of the above-mentioned one chip integrated circuit realizes data transfer of a digital signal delivery system, the signal terminal which control the above-mentioned memory capacity, the signal terminal which output an analog sound signal, the signal terminal which support actuation to

the above-mentioned digital sound signal regenerative circuit, the signal terminal in which the condition of the above-mentioned digital sound signal regenerative circuit is shown, and the signal terminal which supply power to the above-mentioned 1 chip integrated circuit.

[Claim 41] The digital voice regenerative circuit of claim 38 characterized by including the process which carries out the self-test of the defective part of the above-mentioned store circuit, and skips the address of a defective part in the above-mentioned digital sound signal regenerative circuit when writing information in the above-mentioned store circuit, claim 39, or claim 40.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention uses delivering the specified speech information to those who were specified with the gestalt of an electrical signal, and selling thru/or offering it, concerning a digital signal delivery system, a digital sound signal processing circuit, and a signal transformation circuit, for the realized digital signal delivery system, the suitable digital sound signal processing circuit and suitable signal transformation circuit for it, a data compression, and an expanding circuit, and relates to an effective technique.

[0002]

[Description of the Prior Art] there are a newspaper, a journal, etc. which print an alphabetic character etc. through paper since it is old, and are sold as examples of commercialization, such as information. It replaces with the above-mentioned paper and there is also an example which sells various software etc. through the storage like floppy disk memory or an IC card. Moreover, providing with news or a program the specific person who contracted through means of communications like cable television or satellite broadcasting service is also performed.

[0003] Furthermore, unlike the conventional note type personal computer or the electronic notebook, without receiving constraint of time amount and a location, a message is sent to other men or access to a database and the pocket mold computer into which it enabled it to process information simply further are proposed in the page 116 on November 26 "Nikkei electro NISUKU", 1990 - the page 124. this system -- setting -- a pocket mold terminal -- receiving -- a public telephone and FM broadcasting -- letting it pass -- data transmission -- a line -- things, offering an IC card by the bookstore or the kiosk, etc. are proposed.

[0004] Moreover, it is indicated also about the system which performs informational

offer and transfer to JP,63-61391,A.

[0005] Moreover, the digital-to-analog converter realizable [with a digital circuit] is proposed by JP,61-236222,A.

[0006]

[Problem(s) to be Solved by the Invention] performing a deforestation and when it becomes unnecessary, dust makes it discharge in order for printing and transport to take time amount and to make paper for it to to be not only unsuitable for the sale of timely information, but in commercializing and selling information etc. through the paper like a newspaper or a journal -- like -- aggravation of earth environment is brought about. Moreover, when it carries out through an IC card or a FUROPI disk like an electronic notebook, since these terminal units are premised on information processing like an electronic notebook, the actuation is comparatively complicated and they terminal units, such as an electronic notebook and a personal computer, are not only needed, but have barred spread with it. [it is user-unfriendly and common] Moreover, when the data of a large quantity are poured using FM broadcasting, selection of required information will receive by package deal to unnecessary information besides required information like the above-mentioned satellite broadcasting service or cable television broadcasting, and it will not only become troublesome, but is inefficient-like.

[0007] Then, an invention-in-this-application person etc. came to develop the suitable digital sound signal processing circuit for the digital signal delivery system and it which are reproduced by the memory card with a regenerative function of super-** type which can carry the information which made it possible to deliver the information on as [gestalt / of an electrical signal] etc. with the same gestalt as common goods, and was received, and the signal transformation circuit.

[0008] The object of this invention is to offer the digital signal delivery system which realized the sale of the information which had commodity value with the gestalt of an electric digital signal.

[0009] In the above-mentioned digital signal delivery system, other objects of this invention are rates quicker than the signal processed at least, and are to realize delivering a digital signal between the above-mentioned digital signal supply source and the above-mentioned memory card with a regenerative function.

[0010] Furthermore, other objects of this invention are to offer the terminal unit suitable for the above-mentioned digital signal delivery system.

[0011] furthermore, the high quality of the above-mentioned memory card with a regenerative function to which other objects of this invention were suitable for the above-mentioned digital signal delivery system -- ** -- it is in offering the playback approach and equipment. [like]

[0012] Furthermore, other objects of this invention are about an efficient transfer of the information in the above-mentioned digital signal delivery system, and

informational security to offer that approach and equipment.

[0013]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application. That is, in delivery of a digital signal, the microminiature super-** type card-like player which has an earphone as a memory card with a regenerative function corresponding to the terminal unit and one to one as a digital signal supply source is connected, and while making a reception store circuit memorize the specified digital signal with a gestalt as it is, it is reproducing the digital signal made to memorize by the above-mentioned player independent.

[0014] For example, in the above-mentioned digital signal delivery system, a digital signal is delivered at a rate quicker than the signal processed at least between the above-mentioned digital signal supply source and the above-mentioned memory card with a regenerative function. Moreover, while carrying out the reception storage of the digital signal through a communication line or a suitable storage between digital signal supply sources if needed from this supply origin the supply origin of a digital signal, the digital signal which was connected with the above-mentioned memory card with a regenerative function (player) through the connector, and was specified is delivered. Furthermore, the storage capacity of the above-mentioned terminal unit is the same or the storage capacity beyond it compared with the storage capacity of the store circuit on a memory card with a regenerative function (player). The magnetic disk memory equipment which has comparatively big memory capacity in the above-mentioned terminal unit is used as a backup memory. Carrier delivery of efficient information is performed by making the buffer memory constituted by the semiconductor memory in which rapid access is possible memorize the digital signal which delivers between memory cards with a regenerative function, and is updated with a digital signal or the passage of time with many amounts. Furthermore, the storage region to the store circuit in a memory card with a regenerative function is managed. Moreover, the above-mentioned terminal unit realizes the audition with the function to make a part of specified digital signal restrict, reproduce and output to fixed time amount, ****** by silent period control, and the digital signal delivery system that already heard it and had the memory card with a regenerative function of microminiature super-** type by quantizing noise clearance etc. further.

[0015]

[Function] a player comes out as it is and demonstrates worth of the digital signal delivered since a digital signal is reproduced [the gestalt of an electrical signal] by reception and independent -- things can be carried out. Since it is good, while being able to perform the processing, manufacture, and construction of a sale system easily by this with the gestalt of a digital signal, the configuration of a player is easy, and it is a microminiature super-** type card-like, and since actuation is also easy, it can treat

to anyone. [0016] which degrades voice quality by expanding the silent period of a digital sound signal substantially, or making it extend There are nothings, it is already heard and ******** becomes possible.

[Example] The important section block diagram of one example of the digital signal delivery system concerning this invention is shown in drawing 1 . It is turned to the system aiming at commercializing and selling a digital signal in this example. That is, there is a sale of a digital signal as one gestalt of delivery of a digital signal.

[0017] The block diagram of a terminal unit is shown in this drawing among digital signal sale systems. This terminal unit 100 is equivalent to the automatic vending machine of the soft drinks like tobacco or juice. Although this terminal unit 100 plays the role of an information server and is not restricted especially, it connects with the selling agency of a digital signal through broadband digital telecommunication circuit B-ISDN, and reception of the digital signal as goods is performed. A digital signal is made to transmit by taking such a system only to the terminal unit 100 specified by letting a communication line pass like the goods like the above-mentioned tobacco or juice. If it is in the digital signal as goods in this case, there is no cod roe also about traffic congestion or air pollution like conveyance of the common goods like the above-mentioned tobacco or juice, and, moreover, data transfer as goods of a large quantity can be performed at a high speed. The above-mentioned terminal unit 100 is installed in in front of the store [of the firm like a kiosk, a tobacconist's shop, or a bookstore].

[0018] When a terminal unit 100 is roughly divided, it consists of the input section 102, the storage section 103, and the output section 104, each circuit block is connected by VME bus 105, and transfer of a digital signal and various control signals is performed. The memory card 101 (following player) with a regenerative function shown in this terminal unit 100 by the dotted line in this drawing is connected, and the specific digital signal as goods wins popularity as it is, and is passed.

[0019] The block diagram of the input section 102 of the above-mentioned terminal unit 100 is shown in drawing 2 . The input section 102 of the above-mentioned terminal unit 100 has a digital input interface corresponding to broadband digital telecommunication circuit B-ISDN, and the analog input interface (a right analog input, left analog input) which receives the input signal in the gestalt of an analog signal. The excessive frequency band component by which low pass filters 202a and 202b are formed corresponding to the right input Rin and the left input Lin, respectively, and an analog input interface is included in the analog input signals Rin and Lin is removed beforehand. And these input signals Rin and Lin are chosen by turns in time through a multiplexer 203, are incorporated in the sample hold circuit 204, and are changed into a digital signal by an analog / digital conversion circuit 205. At this time, from an analog / digital conversion circuit 205, serially, the digital signal of 2 CHINYANERU (stereo) of a right channel signal and a left channel signal is outputted in time sharing,

and is incorporated by the above-mentioned digital input interface 207. Such an analog input interface digital-signal-izes the music program sent by broadcast etc., a regular news program, stock information, or various commodity markets, and is used for making a store circuit memorize etc.

[0020] In addition, a monophonic signal is inputted using the above-mentioned right or a left input signal. Like a music program, to the large input signal of a band, the band of low pass filters 202a and 202b may be made large, and functions, such as switching narrowly the band of low pass filters 202a and 202b to the narrow input of a band like a news program, may be added. 206 is an input section control circuit and 201 is a network interface corresponding to above-mentioned B-ISDN.

[0021] It connects with the telephone line and you may make it the above-mentioned analog input interface receive the message from an answering machine machine. In this case, a telephone function is added to a terminal unit 100, and you may make it receive the message which connected with the above-mentioned answering machine machine, and was recorded. Thus, if an analog input interface is used, the transfer time of a message will become long. then, two or more messages recorded when digital-signal-izing a message with a digital-type answering machine machine and making it make it memorize, if the subscriber with a digital circuit had -- **** -- it is receivable by short time amount. If it does in this way, in a destination, a message can be caught at the time of the arbitration of the migration middle class by a means of transportation etc.

[0022] The block diagram of one example of the storage section in the above-mentioned terminal unit 100 is shown in drawing 3 . This storage section contains the microprocessor 306 which performs information processing according to ROM (read only memory)307 and the above-mentioned program in which various programs, such as data transfer actuation with the player 101 connected to the display action and the output section of data transfer with external storage like hard disk memory 301 grade, and the information processing program for RAM (random access memory)308 as buffer memory and the above digital inputs, or an analog input and the hard disk memory 301 and a liquid crystal display 303, were stored, and control action. Although especially RAM308 is not restricted, it has the memory capacity of about 1MB, and ROM307 has the memory capacity of about 512KB (it is the same a kilobyte and the following). Especially the hard disk memory 301 plays a role like [although not restricted / have the memory capacity of about 250MB (it is the same a megabyte and the following), and it has a function as a backup memory at the time of power-source cutoff, and also] the warehouse of storing the digital signal of varieties. It connects with an internal bus 309 through the hard disk control circuit 302, and this hard disk memory 301 performs writing and read-out of data according to directions of a microprocessor 306.

[0023] 303 is a liquid crystal display, and it is used in order to display the display of an

information menu, operator guidance, etc. A touch key function is added and the front face performs selection of a display menu, a display switch, etc. For example, if a player 101 is inserted, 1. music, 2. news, 3. weather report, 4. stock quotations, 5. reading, etc. will be displayed as an information menu first displayed on the display screen. And if it specifies, one, for example, 2. news, in it, a screen will change and the display of 1.NHK, 2.FEN, 3. traffic information, 4. sports highlight show, etc. will be performed. And a player 101 receives the digital signal corresponding to it by specifying the news program for which it wishes.

[0024] For example, in the case of 1. music, if a classic, POPYURA, a popular song, and the music genre like jazz are displayed and a specific music genre is chosen, the music name which can be sold will be displayed corresponding to it. Although especially this music information is not restricted, it is made to store in the specific area of ROM307 or the hard disk memory 301. When there is no applicable music in the hard disk memory 301, it connects with a digital signal selling agency through above-mentioned communication line B-ISDN, and is handed over by the player 101 in response to transmission of the target music program. The above-mentioned liquid crystal display 303 is connected to an internal bus 309 through the LCD control circuit 304, and the input of the touch key corresponding to the above displays and they is performed.

[0025] A bus interface 305 is a VME bus interface which makes connection between the above-mentioned internal bus 309 and VME bus 105.

[0026] It is made to make the thing with the need of transposing to the newest information with the passage of time as it was called the above-mentioned news and stock quotations store in the buffer memory 403 prepared in the output section mentioned later. Thereby, it can transmit to a player 101 promptly, without accessing the hard disk memory 301 in detail. Moreover, what has many distribution costs also at a music program is good also as what is stored in buffer memory 403. In this case, as a display menu, corresponding to each music genre, a distribution cost displays the thing of the top ten and may be made to make a user's selection easy.

[0027] The output section of the above-mentioned terminal unit 100 consists of the output interface 401 connected to VME bus 105 as shown in drawing 4 , the player control circuit 402 and buffer memory 403, a monitor control circuit 404, and monitor circuit 405 grade. It has KONETAKU which makes connection with a player 101, it connects with a player 101 through a connector, and the output section delivers the digital signal as goods. This in which buffer memory 403 has the comparatively big storage capacity of about 96MB corresponds about 10 times with a maximum storage capacity [of a player 101] of 8MB which is mentioned later.

[0028] Although not restricted, especially the monitor circuit 405 is equipped with a loudspeaker 406 or a headphone output, and is used for telling the part of SAWARI at the time of song selection of a music program etc. So to speak, this function is a

function called browsing of a bookstore, and when preventing sales promotion of an immaterial digital signal, and the selection mistake of a digital signal, it is effective. Although especially the above-mentioned monitor output function is not restricted, it is made to make only the period whose touch key etc. is an ON state output by making about 10 seconds into the maximum time amount. Since a monitor output is suspended by this as soon as the object is attained, the dead time of monitor playback can be abolished. What has this monitor circuit 405 and its monitor control circuit 404 equivalent to the regenerative circuit of a player 101 mentioned later is used.

[0029] Goods called the tobacco and juice which are sold with an automatic vending machine as mentioned above are put in into a package or a container, and are sold in one with a package and a container. Moreover, the information by which the former was commercialized is sold sure enough in roles [it], such as a package and a container, through the print, floppy, and IC memory through paper. And a music program is also sold in one with storages, such as a magnetic tape and a compact disk. These media have no commodity value in itself. It combines with terminal units, such as an electronic notebook and a personal computer, is carried out, and ejection of the information as goods and processing are performed. Moreover, a music program is also combined with a cassette type tape recorder or a regenerative apparatus, and worth of ****** is demonstrated at the beginning of ****.

[0030] On the other hand, in this application, the digital signal as goods is delivered as it is, without making the storage which plays the role of the above containers intervene. For delivery of such a digital signal, the store circuit 701 mentioned later is carried in a player 101. And playback with player 101 simple substance is enabled by the regenerative circuit in which a player 101 has the digital signal incorporated in this store circuit 701. That is, the goods received and passed demonstrate the value as goods promptly as it is. Such two descriptions differ from dealings of the goods in the former greatly. Moreover, a player 101 is connected to a terminal unit 100 as mentioned above, and only the information required by the way which is the need can be specified and sold in the system which performs delivery for the digital signal as goods.

[0031] in drawing 4 , although 407 is a power circuit and it is not restricted especially, it transmits and the high-speed digital signal to a player 101 puts in another way -- if it becomes, supply of a power source of operation will be performed from a terminal unit 100 for write-in actuation. Moreover, while delivery of the above digital signals is performed [when it replaced with a primary cell which is mentioned later as a power source of a player 101 and the rechargeable battery which can be charged was used, or] when a primary cell and a rechargeable battery are built in, and a player 101 is connected to a terminal unit 100, boosting charge to a rechargeable battery is also performed by the above-mentioned power circuit 407. As an example of the signal delivered and received between the above-mentioned output section and a player 101,

there are above-mentioned operating voltage V, digital signal D, and address signal A, a control signal C, status signal S, etc.

[0032] Moreover, the present cassette tape recorder etc. has equal informational storage time and playback time amount in principle. This poses a big problem to a user in the automatic sale system of information which is proposed by this application. Therefore, in the above-mentioned digital signal delivery system, when a user's user-friendliness is taken into consideration, it is desirable to accelerate delivery of the digital signal between a terminal unit 100 and a player 101 as much as possible. This function is realizable if the control circuit and data transfer means of a store circuit and a store circuit of operating more quickly than the signal reproduced at least are formed in the buffer memory 403 of the terminal unit output section 104 and the store circuit 701 of a player 101 in drawing 4 .

[0033] This example is explained using drawing 5 and drawing 6 . First, drawing 5 is a block configuration about the fast transfer by the side of a player 101. Photosensor 502, the I-V amplifier 503, the serial/parallel-conversion circuit 504, the PLL oscillator circuit 505, the frequency divider 506, the multiplexer 507, and the mode switch 508 are added in the player. since B input side of a multiplexer 507 be choose and it become Y output at the time of optical mode (a mode switch 508 be make into a light side), the external data (the start bit which show the condition of "1" and the condition of "0" be add to the head section of a unit write-in data stream by 2 bits) supply as a pulse train of light will be write in a store circuit 701. That is, a light modulation pulse train is changed into a current signal with photosensor 502, is shaped in waveform as a voltage signal with the I-V amplifier 503, and it is inputted into the serial signal input terminal D of the serial/parallel-conversion circuit 504 at the same time it inputs into the PLL oscillator circuit 505 for extracting a clock component from the pulse train after this plastic surgery. While the clock signal (this application frequency of 8MHz) extracted in the above-mentioned PLL oscillator circuit 505 becomes the shift clock of the above-mentioned serial/parallel-conversion circuit 504, it becomes the count clock of 1 (n is +2 bits in quantifying bit number, and is 10 in this application)/n frequency divider 506, and the output signal (an example 800kHz) of this frequency divider 506 turns into a write-in strobe signal to a store circuit 701.

[0034] Moreover, since A input side of a multiplexer 507 is chosen and it becomes Y output at the time of electric mode (a mode switch 508 is made into an electrical-and-electric-equipment side), 16-bit parallel data will pass a multiplexer 507 from an input buffer 501, and will be written in a store circuit 701.

[0035] The block configuration which shows the data transmitting section by the side of a terminal unit 100 is shown in drawing 6 . 8-bit parallel data outputs the data output of buffer memory 403 by the output buffer 601, and a light modulation pulse makes the data of buffer memory 403 a serial signal in the parallel/serial-conversion

circuit 602, adds 2 bits of start bits which show the condition of "1", and the condition of "0" to the head section of a data stream in the start bit addition circuit 603, with the V-I amplifier 604, it drives a laser diode 605 and outputs it as a pulse train of light.

[0036] According to this example, information, such as a sound signal, can be transmitted to a high speed by the wireless by optical coupling. For example, at this example, the speech information for about 6 minutes (the resolving power of 8 bits, the sampling frequency of 22.05kHz, monophonic recording) was able to be transmitted in only 10 seconds. Moreover, also in the example which set the frequency of a clock signal as 800kHz for the purpose of lessening power consumption at the time of fast transmission, somewhat, although time amount was required, it was able to obtain the good result.

[0037] The basic thought of this example is in the point of transmitting the content of digital memory to a high speed with a direct digital signal, paying attention to being quicker than the analog signal with which the working speed of digital memory, such as semiconductor memory, is processed, and it cannot be overemphasized that many application actuation is possible in the range of this thought. For example, although a direct connector or a cable ties data transfer [not an optical coupling method but] origin, the completely same result may be obtained, and an operation of application of an electric wave or the MAG may be used. Furthermore, by the method which transmits 8-bit parallel data, although the number of pins of a connection connector increased, the about single [more] figure transfer rate was able to become short, and the circuit of a transmitting side or a receiving side was able to transmit the data for about 6 above-mentioned minutes in only 1 second, in spite of having been simplified.

[0038] Moreover, although how the direct terminal unit 100 manages the store circuit 701 of a player 101 was taken in this example The method which terminates a transfer when a transfer is started from the address (zero address) of the beginning of a store circuit 701 and an address counter (for example, 703 of drawing 7 mentioned later) overflows, By adding ID information to the head part of a transfer data stream, the approach of transmitting the data from the address of the arbitration of said store circuit 701 to the address of arbitration at high speed was also able to be checked, and the good result was able to be obtained.

[0039] Usually, consideration of a user's user-friendliness demands to be able to choose a required thing, to transmit to a player 101, and to be able to reproduce to the time amount of arbitration in the location of arbitration repeatedly out of the abundant information accumulated in the terminal unit 100. Therefore, the storage capacity of a terminal unit 100 is the same at least, or becomes more than it from the storage capacity of a player 101. That is, it becomes the relation of Mp<=Ms when storage capacity of Mp and a terminal unit 100 is set to Ms for the storage capacity of a player 101. In addition, especially this condition is not limited depending on an application gestalt. The block diagram of one example of the above-mentioned player

101 is shown in drawing 7 .

[0040] It consists of a large-scale integrated circuit 709 which consists of a store circuit 701 which remembers that a digital signal roughly divides a player 101, a gate array, etc., and a regenerative circuit. Although especially the store circuit 701 is not restricted, it consists of false static molds RAM with the memory capacity of about 8MB. For example, 16 abbreviation 4M bit false static molds RAM (PSRAM) are carried so that it may mention later, and storage capacity of above-mentioned about 8MB is realized. As for a large-scale integrated circuit 709, a control circuit 704, an address counter 703, a multiplexer 702, and the parallel/serial-conversion circuit 705 are carried. the digital signal memorized in the store circuit 701 carries out reading appearance of the control circuit 704, and it also forms the control signal at the time of the data input to the store circuit 701 besides the various control signals at the time of playback actuation.

[0041] An address counter 703 reads the digital signal memorized in the store circuit 701, and generates the address signal at the time. A multiplexer 702 performs the time of accessing a store circuit 701 from a terminal unit 100, and the address switch when accessing a store circuit 701 inside. That is, the writing of the digital signal to a store circuit 701 is performed by the address from a terminal unit 100 side, and read-out at the time of playback actuation of the digital signal is performed by the address generated by the address counter 703.

[0042] 706 is a low pass filter, consists of digital filter circuits and inputs only a band component required for playback into the digital to analog circuit 707. In this example, according to information or a program, the digital signal of two or more sampling rates is treated so that it may mention later. A switch of the passband of a digital filter is also performed according to these sampling rates. A digital to analog circuit has the function which outputs the analog signal of the right-and-left channel divided into right and left corresponding to the stereo signal inputted in time sharing. In addition, when a digital signal is a monophonic signal, the same analog signal is outputted from both channels. A player 101 is made to perform a voice output by headphone for the formation of small lightweight. 711 is a phones jack for it.

[0043] The top view of one example of the mounting substrate which constitutes a player 101 is shown in drawing 8 . A player 101 consists of a control substrate 807 and a memory board 802. The power supply section and connector area which insert the carbon button cells 808a-808d are divided and prepared in the ends of a longitudinal direction, and electronic parts, such as each semiconductor integrated circuit equipment which constitutes the above-mentioned large-scale integrated circuit 709, and the amplifying-circuit component 805,806, a low pass filter 706 and the digital to analog circuit 707 on a substrate front face in the meantime, are carried in the control substrate 807. What doubled the connector 804 with JEIDA (Japan Electronic Industry Development Assosiation: Japan Electronic Industry Development

Association) specification (specification, such as a memory card) is used. A power supply section consists of a carbon button cell holder, for example, four-piece mounting of an alkali carbon button cell (LR44) is enabled. Although not restricted, the receipt especially of the size of this control substrate 807 in the case for the existing IC cards is enabled width being used as 82mm length being used as 52mm.

[0044] A memory board 802 is equivalent to the magnitude except the part corresponding to the connector area and power supply section in the above-mentioned control substrate 807 where thickness is comparatively thick, and every eight PSRAM(s) are carried in both sides. This memory board 802 and the control substrate 807 are connected by the flexible wiring substrate 803. That is, in order to make inspection, repair, etc. easy, the spread of the two above-mentioned substrates is made possible.

[0045] The side elevation of the mounting substrate in the condition of having been stored in the case is shown in drawing 9 . It turns up, when a memory board 802 minds the flexible wiring substrate 803 except the power supply section and connector area of the above-mentioned control substrate 807, and it piles up. Receipt in a case equivalent to the existing IC card (RAM card) is attained by this, and the small and thin player 101 can be realized. Moreover, since it changes into the condition of having opened the memory board 802 and the control substrate 807 as mentioned above at the time of repair, exchange of electronic parts, such as IC and LSI, etc. can be performed simply.

[0046] The top view of other one example of a player 101 is shown in drawing 10 .

[0047] In this example, player 101 body and the store circuit section 1001 are made removable. That is, player 101 body is constituted from an IC of the large-scale integrated circuit 709 for control, the digital-to-analog circuit 707, and amplifying-circuit 708 grade, a cell case, and memory card connector 804 grade of JEIDA specification conformity by the control substrate 807 at said this appearance. And as a dotted line shows, the store circuit section connector 1103 indicated to be the space which can insert the store circuit section 1001 (memory card) of a thin card condition in the interior at drawing 11 is formed in this drawing. The above false static molds RAM and the cell for the backup are stored in a thin card-like plastic case, and the store circuit section 1001 is constituted, for example. Thus, by making the store circuit section 1001 removable, two or more kinds of memory cards can be prepared. as RAM -- the static mold RAM and the dynamic mold RAM -- or what the storage capacity becomes from two or more kinds can be prepared. Moreover, a ROM card can also be used besides the above RAM. It may be made to deliver a digital signal using EEPROM besides the thing using mask type ROM as a ROM card. While taking time amount somewhat compared with delivery of a digital signal, and the case where write-in actuation of a digital signal uses RAM if it puts in another way when such an EEPROM is used, since the cell for backup becomes unnecessary, manufacture of a

memory card and handling become simple.

[0048] Moreover, compatibility with the existing IC memory card is securable by making the above-mentioned JEIDA specification (the current guideline Ver4.0 being standardized) adopted as general-purpose IC memory cards, such as an electric specification, card attribute information, etc., such as physical specifications, such as an appearance of the above-mentioned player 101, and a connector, a signal property, and timing, suit. In addition, although a dimension, a connector, pinout, cell voltage, etc. are standardized by JEIDA specification, the pinout and the signal property of a dimension and a signal are extracted especially in this application. Drawing 63 shows the appearance of the type I card by JEIDA specification. A dimension is 85.6mm. x 54.0mm x It is 3.3mm. Drawing 64 shows the appearance of the type II card by JEIDA specification. A dimension is 85.6mm. x 54.0mm x It is 5.5mm (however, a connector area 3.3mm). drawing 65 -- the pinout of a signal -- being shown -- **** -- a guideline Ver4.0 -- the number of pins -- 68 -- focuses -- **** -- it is. Drawing 66 shows the signal property.

[0049] The block diagram of the player 101 above-mentioned body and one example of the store circuit section 1001 is shown in drawing 11 .

[0050] The memory card connectors 804, such as JEIDA specification conformity connected with the above terminal units 100, are formed in the outside of player 101 body. And the store circuit section connector 1103 is formed in the interior. The store circuit section 1001 of the shape of an above card is made removable through these store circuit section connectors 1002 and 1103.

[0051] The data inputted from the memory card connector 804 corresponding to a terminal unit 100 are supplied to the data input terminal Di of the store circuit section 1001 through the store circuit section connectors 1002 and 1103. The address inputted from the memory card connector 804 corresponding to a terminal unit 100 is supplied to one input A of a multiplexer 1105. The address for playback generated by the address counter 1106 of player 101 body is supplied to the input B of another side of this multiplexer 1105. The address for delivery of a digital signal and the address for playback are selectively supplied to address terminal A of the store circuit section 1001 through this multiplexer 1105. And the control signal inputted from the memory card connector 804 corresponding to a terminal unit 100 is supplied to one input A of a multiplexer 1104. The control signal for playback formed of the control circuit 1101 of player 101 body is supplied to the input B of another side of this multiplexer 1104. The control signal for delivery of a digital signal and the control signal for playback are selectively supplied to the control terminal C of the store circuit section 1001 through this multiplexer 1104.

[0052] Playback of a digital signal performed by accessing by the delivery of a digital signal which forms the above multiplexers 1105 and 1104, performs the change of the address or a control signal, and is performed by accessing the store circuit section

1001 from a terminal unit 100 side, the address counter 1106 of player 101 body, or the control circuit 1101 is performed selectively. In the above-mentioned playback actuation, the digital signal outputted by read-out actuation of the store circuit section 1001 from an output terminal Do is outputted as a sound signal through the regenerative circuit which consists of the low pass filter 706, the digital to analog circuit 707, and amplifying-circuit 708 grade of player 101 body through the store circuit section connectors 1002 and 1103.

[0053] According to the ID code of the digital signal reproduced etc., the above low pass filters 706 are controlled, or the control circuit 1101 of player 101 body performs control of the digital to analog circuit 707 etc.

[0054] Moreover, when the operating voltage for the high-speed writing of the digital signal to the store circuit section 1001 connected through the above-mentioned store circuit section connectors 1002 and 1103 and the cells 808a-808d carried in player 101 body are rechargeable batteries, the power source supplied from a terminal unit 100 is used also in order to perform the boosting-charge actuation.

[0055] The block diagram of one example of the current supply method of a player 101 is shown in drawing 12 . A player 101 is divided into a store circuit 701 and the amplifying circuit 708 which outputs the control circuit 704 which consists of digital circuits, a digital filter 706, the digital to analog circuit 707 which is mentioned later, and an analog signal as mentioned above. These the circuit blocks of each differ in each operating voltage. For example, a store circuit 701 needs the comparatively high operating voltage of about 4v, when using the above false static molds RAM. On the other hand, a digital circuit can operate on about 3 V and a comparatively low electrical potential difference by using a CMOS-circuit gate array etc. And if it is in the amplifying circuit 708 which drives headphone, operating voltage is low better still at about 1.5v. Except for the store circuit 701 where the electrical potential difference of a cell 1203 is regularly given from this using the cells 1203, 1204, and 1205 set by the operating voltage of each circuit for information maintenance actuation, the electrical potential difference of cells 1204 and 1205 is supplied to each circuit which corresponds through electric power switches 1206 and 1207, respectively.

[0056] Thus, a battery life can be lengthened by being made to perform current supply in the circuit which corresponds directly using two or more kinds of cells by which electrical-potential-difference values differ. For example, if an internal electrical power source is doubled with 4V [highest], in a digital circuit or an analog circuit, a useless current will flow and the consumed electric current will increase. Then, if the pressure of the above-mentioned 4V is lowered in an internal pressure-lowering circuit, since current consumption is performed also in a pressure-lowering circuit, a battery life will be shortened after all. On the other hand, in this example, since the cell of need min is chosen as each circuit and current supply is carried out to it, useless current consumption is held down and a substantial battery life can be

lengthened.

[0057] In order to perform write-in/of the digital signal to a store circuit 701, or read-out of a digital signal at a high speed, the operating current of a store circuit 701 becomes large. Then, the connector for current supply is prepared in a terminal unit 100, and operating voltage like about 5 V higher than the above-mentioned internal electrical potential difference is supplied from there. In this case, in order to perform automatically the power-source switch by the side of a player 101 and a terminal unit 100, a connector 804 and a cell 1203 are made to perform electrical-potential-difference supply to the power supply terminal of a store circuit 701 through diodes 1201 and 1202, respectively. With this configuration, if a player 101 is connected to a terminal unit 100, since the operating voltage by the side of a terminal unit 100 is high compared with about 5 V and about 4 V of a cell 1203, diode 1201 will be turned on, and a store circuit 701 will be operated by the operating voltage from a terminal unit 100 side. At this time, the reverse bias of the diode 1202 by the side of a cell 1203 is carried out, it is turned off, and a back run current does not flow from KONETAKU of a terminal unit 100 on a cell 1203. And if a player 101 is sampled from a terminal unit 100, since a connector will be opened, diode 1202 is turned on and the electrical potential difference of a cell 1203 is supplied to a store circuit 701. The battery life of a player 101 can be lengthened performing data transfer from a terminal unit 100 side to a store circuit 701 at a high speed by taking such a current supply method.

[0058] The block diagram of one example of the digital signal transmitted to a player 101 from a terminal unit 100 is shown in drawing 13 .

[0059] what needs a frequency band widely like a music program as the source of a digital signal, and the thing which does not need a frequency band widely like news -- or there are what needs stereophonic reproduction, and what monophonic playback is enough as. Thus, in order to use effectively the memory capacity to which the store circuit 701 built in a player 101 according to the source was restricted, as a digital signal, selection of a sampling rate, bit length, and a stereo/monophonic recording is enabled according to the source. When it does in this way, setting out of the playback conditions which corresponded for every source is needed. In this case, the display means for directing selection, if it is made to choose with hand control increases, and if it does not get used to treatment, tone quality will deteriorate extremely by the mismatch of playback conditions to the source, or it becomes playback impossible.

[0060] In order to solve such a problem, ID code 1308 which specifies playback conditions as the head of a digital signal as shown in drawing 13 is inserted. The data which consist of a digital signal reproduced following this ID code 1308 are prepared. thus, it is ** as ID code 1308 which directs a digital signal and its playback condition is delivered to a player 101 as a signal of one. Thereby, ID code 1308 and a digital signal are memorized as one in the store circuit 701 of a player 101. For example, in taking

the method which dissociates with a digital signal and transmits ID code 1308 to a player 101, when the power source of a player 101 is intercepted, it needs a device to which ID code 1308 does not disappear, but when a store circuit 701 is made to memorize a digital signal in one like the above-mentioned example, such a problem does not arise.

[0061] As for drawing 14 , the block diagram of one example of the player 101 corresponding to the digital signal with which above-mentioned ID code 1308 is inserted is shown.

[0062] It is considered that the digital signal by which reading appearance is carried out to the beginning from a store circuit 701 is ID code 1308, and it is incorporated by the register 1401. Among ID codes 1308 incorporated by this register 1401, 1300 (D0) and 1301 (D1) are inputted into a multiplexer 1404, choose the clock pulse corresponding to a sampling rate among four kinds of clock pulses formed of the clock generation circuit 1403, and tell it to a control circuit 704. The clock generation circuit 1403 forms four kinds of clock pulses corresponding to a sampling rate in response to the reference frequency signal formed of the oscillator circuit OSC.

[0063] Moreover, 1302 (D2) is inputted into the bit length conversion circuit 1405. The bit length conversion circuit 1405 has a parallel/serial-conversion function, and inputs into a low pass filter 706 the digital signal outputted from a store circuit 701 in a maximum of 2 bytes of unit according to the bit length specified by 1302 (D2). A low pass filter 706 consists of digital filter circuits, and cuts the excess and frequency band of an input digital signal in response to the clock pulse corresponding to a sampling rate from a control circuit 704. Moreover, the digital to analog circuit 707 changes an input digital signal into an analog signal from a control circuit 704 in response to the clock pulse corresponding to a sampling rate. An amplifying circuit 708 amplifies the changed analog signal, and forms the driving signal of headphone etc. In addition, although omitted in this drawing, the low pass filter which consists of resistance, a capacitor, etc. is prepared in the output section of the digital to analog circuit 707.

[0064] Although especially ID code 1308 is not restricted, it consists of 8 bits (1 byte) of 1300-1307 (D0-D7), for example, assignment of four kinds of sampling frequencies is performed by 1300 and 1301 (D0 and D1). 44.1kHz is specified, if 1300 and 1301 are 00, 5.5125kHz, and 1300 and 1301 are 01, 11.025kHz, and 1300 and 1301 are 10 and 22.05kHz, and 1300 and 1301 are 11. 1302 is used for assignment of resolving power, and 16 bits is specified, if it is 0 and is 8 bits and 1. And 1303 (D3) is used for mode assignment, and if it is 0 and it is a monophonic recording and 1, it is used as a stereo. And it has left the 4 bit 1304-1307 (D4-D7) remaining to extension.

[0065] Here, the memory space (total number-of-bits M) of a store circuit 701 and the relation between bit length N as resolving power, a sampling rate fs and Mode S (it considers as a stereo S= 2 and a monophonic recording S= 1), and the record playback

time amount t are expressed by the degree type (1).

[0066]

t=M/(NxfsxS) ..... (1)

As the above-mentioned sampling rate, although not restricted especially, 44.1kHz is used for playback of the music program of super-HiFi equivalent to a compact disc player, 22.05kHz is used for playback of a HiFi music program, 11.024kHz is used for playback of information programs, such as news, and 5.5125kHz is used for playback of an answering machine machine etc. If a sampling frequency is set up every 2 times as mentioned above, as a player 101, one reference frequency corresponding to 44.1kHz is formed, and it can form easily by carrying out dividing of it every [2 / 1/]. Therefore, it is inversely proportional to four kinds of above sampling frequencies fs, and regeneration time amount becomes long. If it puts in another way, when acquiring fixed record playback time amount, storage capacity increases in proportion to a sampling rate fs.

[0067] In the case where bit length is with 8 bits and 16 bits, record playback time amount doubles so that clearly from the above-mentioned formula (1). If bit length is made to increase, corresponding to it, the storage capacity of a store circuit 701 will 2 double be necessary. On the other hand, if bit length is reduced to 8 bits, in the thing of the same storage capacity, regeneration time amount will be expanded twice. And in stereo mode, twice as many data as this are needed compared with monophonic mode. That is, since a right signal and a left signal are outputted by turns from a store circuit 701 at the time of stereo mode, twice [at the time of monophonic mode] as many storage capacity as this is needed.

[0068] In this example, the storage capacity of the limited store circuit can be used effectively for the maximum by setting up the above sampling rates, bit length, and three kinds of playback conditions in the mode corresponding to the source of a digital signal, and making it refreshable at arbitration combining it. And although various combination is made for the variety by these playback conditions, since it can be automatically set as a player 101 using ID code 1308, there is no troublesomeness of actuation and playback of the information which won popularity to anyone simply and was passed is attained.

[0069] The class or frequency of the above-mentioned sampling rate is made to arbitration. In this case, what is necessary is making it just generate a clock pulse according to each sampling rate. And ID code 1308 may add the bit which can be specified by actuation of a terminal unit. For example, the above-mentioned remaining bit may be made to perform automatic setting in ****** mode which is mentioned later, or the already heard mode, or automatic assignment of the playback mode of reproducing the playback and all the programs in a program unit continuously may be performed.

[0070] The circuit diagram of one example of a quantizing-noise clearance circuit is

shown in drawing 15 .

[0071] Digitization of an analog signal surely generates a quantizing noise (error component). This quantizing noise will become jarring especially at the time of silent. In this example, the following quantizing-noise clearance circuits are established in the input section of the digital to analog circuit 707.

[0072] The digital signal by which reading appearance was carried out from the store circuit 701 is inputted into the digital to analog circuit 707, and is changed into analog signal Vout here. Although not restricted especially, the quantizing noise clearance circuit of this example is turned when a digital signal is constituted by the two's complement code. The digital signal which consists of D0-Dn by which reading appearance was carried out from the above-mentioned store circuit 701 is inputted into the input terminals D0-Dn with which the digital to analog circuit 707 corresponds through AND circuits 1510-151n. The level judging the level judging circuit 1507 as showed the digital signal by which reading appearance was carried out from the above-mentioned store circuit 701 in this drawing with the broken line considers that is silent is performed. The output signal of this level judging circuit 1507 consider that is silent is inputted into the timer circuit 1508 shown in this drawing with the broken line, and a time amount judging is performed. If the level the above-mentioned level judging circuit 1507 and a timer circuit 1508 consider that is silent carries out fixed time amount continuation, the output signal which was judged to be a silent period and let the logical negation circuit 1505 pass will serve as logic 0, and it will control to close the above-mentioned AND circuits [1510-151n] gate. That is, AND circuits 1510-151n set compulsorily the input signals D0-Dn inputted into the digital to analog circuit 707 by the logic 0 of the output signal of the above-mentioned logical negation circuit 1505 as logic 0 regardless of the digital signal by which reading appearance is carried out from a store circuit 701.

[0073] Digital signals D0-Dn are constituted by the two's complement code as mentioned above. Namely, when D0-Dn consist of 8 bits, by 01111111, negative maximum is set to 10 million and, as for 0 level, forward maximum is set to 00000000. In addition, +1 of decimal system is 00000001 in the above-mentioned binary system, and -1 of decimal system turns into 11111111 in the above-mentioned binary system. Therefore, if judged with a silent period as mentioned above, the quantizing noise in a silent period can be thoroughly omitted by fixing an AND circuits [1510-151n] output to 0.

[0074] Setting out of forward maximum +deltaL consider that is [the level judging circuit 1507 of this drawing] silent, and negative maximum-deltaL is enabled. +1 [for example,] -- forward maximum +deltaL -- if it carries out, as for the input B of a comparator 1501, 00000001 will be inputted, and 11111111 will be inputted into the input B of a comparator 1509 if -1 is set to negative maximum-deltaL. The digital signal from the above-mentioned store circuit 701 is inputted into the input A of these

comparators 1501 and 1509. A comparator 1501 forms the output signal of 1 at the time of A<=B, and a comparator 1509 forms the output signal of 1 at the time of A>=B. The output signal of these comparators 1501 and 1509 is outputted through AND circuit 1502. So, the output of AND circuit 1502 outputs [a digital signal] 1 of silent detection at the time of 00000001, 00000000, and 11111111.

[0075] In addition, like 00000010 in a digital signal, when larger than +deltaL, the output of a comparator 1501 is set to 0, and like 11111110 in a digital signal, when smaller than -deltaL, the output of a comparator 1509 is set to 0. thereby -- the digital signal from AND circuit 1502 -- the above -- only when it is that it is silent within the limits of ****** level, the output signal of 1 is formed.

[0076] A timer circuit 1508 consists of a counter circuit 1503 and a comparator 1504. The detection output of the above-mentioned level judging circuit 1507 is inputted into reset input [of a counter circuit 1503] R. since reset of a counter circuit 1503 will be canceled if a silent condition is judged -- a counter circuit 1503 -- counting of a clock pulse CK -- actuation is started. counting of a counter circuit 1503 -- an output is supplied to the input A of a comparator 1504. The setup time t for regarding it as a silent period to the input B of a comparator 1504 is inputted. Thereby, a comparator 1504 will set an output signal (A>=B) to 1, if silent level continues and the above-mentioned setup time t is exceeded. Since a logical negation circuit 1505 is reversed and this output signal is inputted into above-mentioned AND circuits 1510-151n, let the digital signal supplied to the input of the digital to analog circuit 707 regardless of the digital signal by which reading appearance is carried out from a store circuit 701 be 0 level of 00000000.

[0077] When the level on which a digital signal exceeds the above-mentioned **deltaL is inputted, a comparator 1501 or 1509 detects it, sets an output to 0, and makes the counter circuit 1503 of a timer circuit 1508 reset in the level judging circuit 1507. Since the output signal of the comparator 1504 of a timer circuit 1508 is set to 0 and an AND circuits [1510-151n] control input is set as 1 through a logical negation circuit 1505 by this, the digital signal by which reading appearance was carried out to the input of the digital to analog circuit 707 from the store circuit 701 is inputted. Thus, termination of a silent period changes into an analog signal the digital signal by which reading appearance was promptly carried out from the store circuit 701.

[0078] According to the experimental result in an invention-in-this-application person, the setup time t of the above-mentioned timer circuit 1508 changes with contents, such as a music program and the news program, but generally the time amount for 0.5ms - about 20ms is desirable. Of course, a big problem is not produced even if it sets it as the time amount which exceeds range [this] somewhat. Moreover, even if the level consider that is silent can be switched corresponding to the input source or its resolution, it is good. For example, it is desirable to set up the range greatly compared with the case of a 8-bit digital signal generally in the case of a 16-bit digital

signal. Moreover, a digital signal does not need to use a two's complement code and, in the case of 8 bits, may make 01111111 or 10 million alternating current middle point level. What is necessary is to replace with a digital signal from a store circuit 701, and just to make it switch to 01111111 or 10 million, when it considers as such a digital signal, if a multiplexer and a gate circuit combine with the input of the digital to analog circuit 707 and a silent period is detected.

[0079] The wave form chart for drawing 16 to explain the above actuation is shown. The case where the wave of 1600a of this drawing inputted the digital signal from a store circuit 701 into the digital to analog circuit as it was, and an analog signal is formed is shown. since signal change is performed in a silent period corresponding to a part for a quantization error as shown in this drawing, it is jarring as a noise -- a basis -- **** -- it keeps. On the other hand, in the quantizing noise clearance circuit of this example, the level consider that is silent as shown in this drawing 1600b is outputted until the next sound signal of 0 level from which the above-mentioned noise was removed comes, since the digital to analog of the digital signal corresponding to 0 level will be compulsorily carried out by 1510-151n of AND circuits, if only a fixed period t passes. between [t] up Norikazu scheduled time -- above -- 0.5ms - about 20ms and **** -- since it is short, the quantizing noise outputted between them will not become jarring

[0080] The quantizing noise clearance circuit 1500 of this example can be widely used as various kinds of digital speech processing circuits, such as what treats a digital sound signal like a digital audio tape recorder besides what is used for the above players 101.

[0081] The circuit diagram of one example of a security circuit used for the digital signal sale system concerning this invention is shown in drawing 17 .

[0082] In selling the digitized speech information as goods, it becomes important, when raising the commodity value to prevent copying it simply. Then, the function that only a specific person is made to perform playback actuation of a substantial digital signal to the 1st is added. If the digital signal sold to the 2nd in the digital signal sale system of said example is transmitted to a player 101, the function for the following signal transformation to be performed inside a player 101, and to prevent an easy copy will be added.

[0083] In order to perform playback actuation of only the above-mentioned specific person, or in order to permit the copy by the specific person, the exclusive "or" circuits 1700-170n controlled by the judgment signal of a password are established in the read-out output section of a store circuit 701. Although these exclusive **** circuits 1700-170n are formed corresponding to all the bits of the read-out signals D0-Dn, they are good also as what forms the above-mentioned exclusive "or" circuits 1700-170n only to others, 1 which contains 1 bit of high orders at least, or two or more bits.

[0084] The digital signal transmitted from said terminal unit 100 (server) is inputted into the input data terminal of the above-mentioned store circuit 701 as it is. In addition, when the semiconductor memory by which the input and output of a store circuit 701 were communalized is used, the above-mentioned exclusive "or" circuits 1700-170n are inserted in a read-out signal path to the signal bus to which the data terminal of a memory circuit is connected. Read-out of a digital signal is performed by the address signal by which the store circuit 701 was generated with the address counter 702 which receives the renewal pulse of the address.

[0085] The above-mentioned password is beforehand set to the player 101 by the switch or ROM. This password is told to a purchaser in the purchase case of a player 101. So, when reproducing a digital signal by the player 101, the above-mentioned password is set. Coincidence of the password registered by the comparator which is not illustrated and the entered password sets a password judging signal to 0. So, an input of 0 which corresponded with 0 outputs the coincidence signal of 0. An input of 1 of the above 0 and an inequality outputs the inequality signal of 1. Thus, when a password judging signal is 0, the exclusive **** circuits 1700-170n carry out through [of the input digital signal] as it is, and are made to output.

[0086] On the other hand, if judged with the password registered by the comparator which is not illustrated and the entered password being inharmonious, a password judging signal will be set to 1. So, an input of 1 which corresponded with 1 outputs the coincidence signal of 0. An input of 0 of the above 1 and an inequality outputs the inequality signal of 1. Thus, when a password judging signal is 1, the exclusive **** circuits 1700-170n reverse an input digital signal, and are made to output. If exclusive "or" circuits 1700-170n are formed to the digital signal of all bits as mentioned above, it will become the sound signal which does not make semantics even if all bits are reversed and carry out analogue conversion of the reversed bit, when a password is an inequality, and an informational security protection will be performed. Moreover, if it puts in another way also when copying, also when outputting the data of a store circuit 701 outside, an easy copy can be prevented by needing a password.

[0087] There is what has not not much important making it into secrecy like news or traffic information. In such a case, it is good also as what is made into the invalid of a password using said ID code 1308. If it puts in another way, only when you need secrecy with ID code 1308, on condition that coincidence of a password, it may be made to perform said security actuation. If it does in this way, it is a sale side and a thing with the need of securing from can be specified. Moreover, when an answering machine is received, there is a case where it should not be asked to others. In such a case, it is good also as what assignment of the security by ID code 1308 makes possible so that a terminal unit 100 may perform the above-mentioned security. Anyway, only when securing from truly with ID code 1308, the troublesomeness of actuation can be made into min by needing the input of a password.

[0088] The circuit diagram of other one example of a security circuit used for the digital signal sale system concerning this invention is shown in drawing 18 . In this example, the security circuit which used the coincidence judging signal and exclusive "or" circuits 1800-180n of a password is established in the data input terminal side of a store circuit 701. Even in this case, since it is changed into the sound signal which the bit of each bit of the digital signal itself written in a store circuit 701 or 1 thru/or arbitration is reversed, and does not make semantics when a password is an inequality, it can secure from to said this appearance. In this case, only when a transfer of the digital signal which needs security from a terminal unit 100 is performed and it is [a password is entered by the touch key of a terminal unit 100 etc. and] in agreement, an effective data transfer is performed substantially, and when it is an inequality, the digital signal which is made to reverse a bit as mentioned above and does not have semantics substantially is made to transmit. It is good also as what it replaces [what] with this and stops the transfer operation itself.

[0089] The circuit diagram of one example of further others of a security circuit used for the digital signal sale system concerning this invention is shown in drawing 19 . In this example, the security circuit which used the coincidence judging signal and exclusive "or" circuits 1900-190m of a password is established in the address input terminal side of a store circuit 701. In this case, when a password is an inequality, unlike the time of the address selection of a store circuit 701 being an input, at the time of an output, it will change to the discontinuous address by reversing 1 thru/or two or more bits to the address with which it continued at the time of an input. Consequently, since the digital signal by which reading appearance is carried out with such the discontinuous address becomes what does not make semantics as speech information any longer, it can be secured from to said this appearance.

[0090] It is good also as a configuration which prepares the security circuit which used 1 thru/or two or more exclusive "or" circuits for each of the both sides of the data and address combining the example of drawing 17 or drawing 18 , and the example of drawing 19 . If it does in this way, the combination of data and its address can perform still higher security.

[0091] The circuit diagram of one example of further others of a security circuit used for the digital signal sale system concerning this invention is shown in drawing 20 . This example is mainly turned to the anti-copying of a digital signal. Each password is registered into the player 101 by EPROM etc. Let this password be the code code it is not told that the purchaser of a player 101 itself is.

[0092] Each bit of these code codes is supplied to one [the exclusive "or" circuits 2000-200n established in the input and output of a store circuit 701, respectively, and] input (2010-201n). Although he is trying to be prepared in an exclusive "or" circuit to all the bits of the data input and data output of a store circuit 701 in this drawing, it is good also as what prepares exclusive "or" circuits 2000-200n and

2010-201n only to 1 thru/or two or more bits of arbitration. However, as for a corresponding input and a corresponding output, the above-mentioned exclusive "or" circuits 2000-200n and 2010-201n are prepared in each as a couple.

[0093] Through [of the data input bit by which exclusive "or" circuits 2000-200n and an input (2010-201n) were set to 0 with the above-mentioned password] is carried out as it is, it is written in, and the data input bit by which exclusive "or" circuits 2000-200n and an input (2010-201n) were set to 1 with the password is reversed and written in.

[0094] the digital signal by which reading appearance was carried out from the store circuit 701 -- the above -- by letting the exclusive "or" circuits 2000-200n controlled by the same password, and 2010-201n pass, as mentioned above, a through bit serves as through as it is, and since it is reversed again, the reversed bit is returned. Since the same digital signal as an input digital signal is told by this to the digital to analog circuit 707, it is carried out to voice playback satisfactory.

[0095] On the other hand, the very thing is made to output read-out of a store circuit 701 to the connector side of a player 101. If it puts in another way, the digital signal by which bit conversion was carried out with the password by the write-in circuit side will be made to output. Thereby, since the copied digital signal becomes what does not make semantics unlike the digital signal of a basis, substantial anti-copying becomes possible. In addition, decode of the above-mentioned password can be performed comparatively easily, if it is a person with the information of a digital circuit. However, considering the selling prices, such as the above news, and stock quotations or a music program, the way of the effort which destroys the above-mentioned security will become high in cost, and semantics will not be made. That is, the security in the digital signal sale system of this application is enough if an easy copy and easy tapping can be prevented.

[0096] The circuit diagram of one example of further others of a security circuit used for the digital signal sale system concerning this invention is shown in drawing 21 . This example is replaced with what performs through/reversal of the bit by the above exclusive "or" circuits, and the rearrangement circuit 2101 is used for it. For example, the thing to which the rearrangement circuit 2101 has two signal paths, and one makes an input signal output as it is, and other one are what the output side bits D0-Dn are spatial to the input-side bits D0-Dn, and performs ****, and a thing to which the least significant bit D0 is made to output as the most significant bit Dn, or D1 is made to specifically output as D2. If a password judging signal is inharmonious, it is made to destroy and output to what does not make semantics [a digital signal] by performing the above-mentioned rearrangement. This rearrangement circuit 2101 is good also as what replaces with the exclusive "or" circuit of drawing 18 , and is prepared in input-side data, and good also as what replaces with the exclusive "or" circuit of drawing 19 , and is prepared in an address input side.

[0097] The concrete circuit diagram of one example of the rearrangement circuit 2101 where drawing 22 is used for the above-mentioned security circuit is shown.

[0098] The rearrangement circuit for 1 bit is shown in this drawing in instantiation as a representative to the digital signal which consists of two or more bits.

[0099] Any one is chosen by the change-over circuit 2201, and the two or more bits input digital signal which consists of D0-Dn is outputted as the least significant bit D0 from an output terminal. The change-over circuit 2201 chooses one from D0-Dn with the selection signal formed of the decoder 2202, and is made to output.

[0100] When the above-mentioned digital signals D0-Dn are 8 bits, in the random-number circuit 2204, the random number (it is 0-7 at decimal system) of a triplet is generated, and the input terminal B of mull IPUREKUSA 2203 is supplied. The binary signal (000) of the triplet which specifies 0 of the decimal system corresponding to the above-mentioned output bit D0 is inputted into the input terminal A of another side of this mull IPUREKUSA 2203. And a password judging signal is inputted into the selection terminal S of mull IPUREKUSA 2203. A password judging signal serves as logic 0, when a password is in agreement, and it sends out the signal of the input A of mull IPUREKUSA 2203 from an output Y.

[0101] Since 0 of the decimal system corresponding to the output bit D0 is inputted into a decoder 2202 through mull IPUREKUSA 2203 when a password is in agreement as mentioned above, a decoder 2202 forms and supplies the selection signal of the input bit D0 to the change-over circuit 2201. Thereby, in the change-over circuit 2201, an input signal D0 is outputted as it is as an output signal D0. On the other hand, when a password is an inequality, the signal of the triplet generated by the random-number circuit 2204 is chosen, and it is inputted into a decoder 2202. Thereby, a decoder 2202 decodes the signal of a triplet and forms one selection signal out of the 8-bit input signals D0-Dn. The probability for the above-mentioned input signal D0 to be chosen is 1/8. Since the circuit same also about the 7-bit remaining output signals as the above is prepared, the probability for input signals D0-Dn to be outputted as they are even when a password is inharmonious becomes very low like 1/(8x8x8x8x8x8x8x8) =1/16777216, and security becomes possible. Since the combination of a bit put in and changed changes with random-number circuits 2204 each time, the description of this circuit can make it impossible substantially to decode true data from the outputted bit string.

[0102] Next, the example of the function which prevents from reading more correctly than the exterior the digital signal memorized at the anti-copying 701 of a digital signal, i.e., the store circuit of a player 101, is explained. Usually, as for the data terminal (D of drawing 4) of a player 101, the input and the output are made to serve a double purpose. and the output enable signal for boiling and making a data terminal into an output state is given. That is, although especially logical level is not limited, only when a player 101 has an effective output enable signal (this application logic 1), a data

terminal will be in an output state. Therefore, although especially an anti-copying circuit is not limited, it is inserted in the part related to the read-out path of data.

[0103] The circuit diagram of one example of a security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention is shown in drawing 23 . In order to permit the copy by the specific person, AND circuit 2301 which controls the output enable signal OE by the judgment signal of a password, and the buffer circuits 23000-2300n where an output is controlled by the output enable signal OE are established in the read-out output section of a store circuit 701. These buffer circuits 23000-2300n maintain an output at a hi-z state, unless a control input becomes logic 1. Usually, these buffer circuits 23000-2300n are formed corresponding to all the bits of the read-out signals D0-Dn.

[0104] The digital signal transmitted from the above-mentioned terminal unit 100 is inputted into the input data terminal of the above-mentioned store circuit 701 as it is. In addition, when the semiconductor memory by which the input and output of a store circuit 701 were communalized is used, the above-mentioned buffer sum circuits 23000-2300n are inserted in a read-out signal path to the signal bus to which the data terminal of a memory circuit is connected. Read-out of a digital signal is performed by the address signal generated by the above-mentioned address counter 703 which does not illustrate a store circuit 701. Moreover, the output enable signal OE is inputted into AND circuit 2301 with the judgment signal of a password, and is controlled by the signal which reversed the password judging signal in the logical negation circuit 2302.

[0105] The above-mentioned password is beforehand set to the player 101 by the switch or ROM. This password is told to a purchaser in the purchase case of a player 101. So, when reading the digital signal memorized by the player 101, the above-mentioned password is set. If the password registered by the comparator which is not illustrated and the entered password are in agreement, it will be inputted into AND circuit 2301, after a password judging signal is made into logic 0 and reversed in a logical negation circuit 2302. So, AND circuit 2301 outputs logic 0, when the output enable signal OE is logic 0, and when the output enable signal OE is logic 1, it outputs logic 1. Thus, when a password judging signal is logic 0, control of buffer circuits 23000-2300n is enabled with the output enable signal OE.

[0106] On the other hand, it is inputted into AND circuit 2301, after a password judging signal will be made into logic 1 and will be reversed in a logical negation circuit 2302, if judged with the password registered by the comparator which is not illustrated and the entered password being inharmonious. So, even if the output enable signal OE is logic 0 and AND circuit 2301 is logic 1, it outputs logic 0. Thus, when a password judging signal is logic 1, regardless of the output enable signal OE, a buffer circuits [23000-2300n] output is made into a hi-z state. Therefore, when outputting the data of a store circuit 701 outside, an easy copy can be prevented by needing a password.

[0107] The circuit diagram of other one example of a security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention is shown in drawing 24 . In this example, AND circuits 24010-2401n which control the output of a store circuit 701 by the judgment signal of a password, and the buffer circuits 24000-2400n where an output is controlled by the output enable signal OE are established in the read-out output section of a store circuit 701. Even in this case, a copy can be prevented to said this appearance with the inequality judging signal of a password. In addition, it can guess easily that 1 bit of data thru/or the bit of arbitration are applicable from this example in this case, it changes to an AND circuit, and an OR circuit, an exclusive "or" circuit, etc. can be used.

[0108] The circuit diagram of one example of further others of a security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention is shown in drawing 25 . The security circuit where the coincidence judging signal and AND circuits 25000-2500m of a password were used for this example is established in the address input terminal side of a store circuit 701. In this case, when a password is an inequality, unlike the time of the address selection of a store circuit 701 being an input, at the time of an output, it will change to the discontinuous address to the address with which it continued at the time of an input by fixing 1 thru/or two or more bits to logic 0. Consequently, since the digital signal by which reading appearance is carried out with such the discontinuous address becomes what does not make semantics as right information any longer, it can be secured from to said this appearance. In addition, it can guess easily that 1 bit of an address input thru/or the bit of arbitration are applicable from this example as well as the example shown in drawing 24 , it changes to an AND circuit, and an OR circuit, an exclusive "or" circuit, etc. can be used.

[0109] The circuit diagram of one example of further others of a security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention is shown in drawing 26 . This example is replaced with what controls the bit by the above AND circuits, and is rearranged like the example of drawing 21 , and a circuit 2101 is used for it. For example, the thing to which the rearrangement circuit 2101 has two signal paths, and one makes an input signal output as it is, and other one are what the output side bits D0-Dn are spatial to the input-side bits D0-Dn, and performs ****, and a thing to which the least significant bit D0 is made to output as the most significant bit Dn, or D1 is made to specifically output as D2. If a password judging signal is inharmonious, it is made to destroy and output to what does not make semantics [a digital signal] by performing the above-mentioned rearrangement.

[0110] The concrete circuit diagram of one example of the rearrangement circuit 2101 as drawing 22 used for the above-mentioned security circuit where drawing 27 is the same is shown.

[0111] The rearrangement circuit for 1 bit is shown in this drawing in instantiation as a

representative to the digital signal which consists of two or more bits.

[0112] Any one is chosen by the change-over circuit 2201, and the two or more bits input digital signal which consists of D0-Dn is outputted as the least significant bit D0 from an output terminal. The change-over circuit 2201 chooses one from D0-Dn with the selection signal formed of the decoder 2202, and is made to output.

[0113] When the above-mentioned digital signals D0-Dn are 8 bits, in the random-number circuit 2204, the random number (it is 0-7 at decimal system) of a triplet is generated, and the input terminal B of mull IPUREKUSA 2203 is supplied. The binary signal (000) of the triplet which specifies 0 of the decimal system corresponding to the above-mentioned output bit D0 is inputted into the input terminal A of another side of this mull IPUREKUSA 2203. And a password judging signal is inputted into the selection terminal S of mull IPUREKUSA 2203. A password judging signal serves as logic 0, when a password is in agreement, and it sends out the signal of the input A of mull IPUREKUSA 2203 from an output Y.

[0114] Since 0 of the decimal system corresponding to the output bit D0 lets it pass mull IPUREKUSA 2203 and is inputted into a decoder 2202 when a password is in agreement as mentioned above, a decoder 2202 forms and supplies the selection signal of the input bit D0 to the change-over circuit 2201. Thereby, in the change-over circuit 2201, an input signal D0 is outputted as it is as an output signal D0. On the other hand, when a password is an inequality, the signal of the triplet generated by the random-number circuit 2204 is chosen, and it is inputted into a decoder 2202. Thereby, a decoder 2202 decodes the signal of a triplet and forms one selection signal out of the 8-bit input signals D0-Dn. The probability for the above-mentioned input signal D0 to be chosen is 1/8. Since the circuit same also about the 7-bit remaining output signals as the above is prepared, the probability for input signals D0-Dn to be outputted as they are even when a password is inharmonious becomes very low like 1/(8x8x8x8x8x8x8x8) =1/16777216, and security becomes possible. Since the combination of a bit put in and changed changes with random-number circuits 2204 each time, the description of this circuit can make it impossible substantially to decode true data from the outputted bit string.

[0115] The circuit diagram of one example of further others of a security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention is shown in drawing 28 . This example is rearranged like the example of drawing 26 , and uses a circuit 2801 for an address input. Moreover, the concrete circuit diagram of one example of the same rearrangement circuit 2801 as drawing 27 used for drawing 29 in the above-mentioned security circuit is shown. Except that, as for this example, the bit length of the data and address differs as compared with the example of drawing 26 and drawing 27 , the concept is completely the same.

[0116] ****** in the quality of loud sound and the block diagram of one example of the digital sound signal processing circuit which realized ****** playback are shown in

drawing 30 .

[0117] In the above digital signal sale systems, in order to perform listening comprehension by the short time, information, such as news and various market conditions, is already heard, and is confirmed by playback. Moreover, when the user of a player is an old man etc., in order for an understanding of about lowering of hearing and the language itself to only take time amount, to add a ****** function is confirmed.

[0118] With analog-type sound recording equipment, such as the conventional cassette tape recorder, ****** and ****** can be performed by changing playback time amount for a tape speed to sound recording time amount. However, if a tape speed is changed in this way, as a result of a pitch's (frequency's) also changing simultaneously and losing the fidelity over a fundamental tone, it will be heard dramatically and will become that of ** potatoes.

[0119] Then, changing reproduction speed, without changing the above-mentioned pitch is also considered by using the signal-processing technique using a digital signal processor etc. However, if it does in this way, while a configuration will become complicated, power consumption will also increase and about [that it cannot carry in the above pocket players] or a price will also become expensive. Furthermore, there is effectiveness only in voice and playback of a music program becomes difficult.

[0120] The silent period included in speech information in this example is utilized, it is already heard, and they are compaction thru/or the thing delete substantially and reproduce, and expand thru/or extend [thing] and it is made to reproduce a silent period at the time of ****** playback about a silent period at the time of playback. By taking such a method, it is already heard, and also in ******** playback, since the pitch of a fundamental tone itself is changeless, it can maintain the quality of loud sound. And the combination of a comparatively easy logical circuit can constitute the configuration so that it may mention later, it does not need to use expensive and complicated equipments, such as a digital-signal-processing processor, and the miniaturization of it is attained cheaply.

[0121] The example in which the example of above-mentioned drawing 30 was carried in the player 101 of said digital signal sale system is shown.

[0122] The digital sound signal by which reading appearance was carried out from the store circuit 701 is inputted also into the silent period detector 3002 while it is inputted into the digital to analog circuit 707. The same circuit can be used for this silent period detector 3002 as having been used for the quantizing-noise clearance circuit 1500 of the example of said drawing 15 drawing. When said quantizing-noise clearance circuit 1500 is also carried, it may common-use-ize with it and the silent period detector 3002 may be used. The output signal of this silent period detector 3002 is already heard, and is inputted into the /****** circuit 3003. It is already heard, and the /****** circuit 3003 is already heard in response to the control signal in the

mode 1 and the mode 2, or assignment of ****** is performed. This motion control of the address counter 703 with which the /****** circuit 3003 forms the read-out address signal of the above-mentioned store circuit 701 to the above-mentioned mode signal by already hearing it is performed. For example, if ****** is specified by the mode 1, and a silent period is detected, by making the frequency of a clock quicker than usual and **(ing) read-out of the store circuit 701 in a silent period, a silent period will be shortened substantially, and will already be heard and it will consider as playback.

[0123] On the contrary, if ****** is specified by the mode 2, and a silent period is detected, it will consider as ****** playback by carrying out a fixed period halt of the frequency of a clock later than usual, and making the read-out time amount of the store circuit 701 in a silent period expand thru/or extend. In addition, the output signal of an address counter 703 is inputted into a store circuit 701 through a multiplexer 702. A multiplexer 702 makes an external address signal input into a store circuit 701, when writing in a digital signal to a store circuit 701, and if it puts in another way when reading the digital signal memorized by the memory circuit, it will make the address signal generated by the address counter 703 at the time of playback actuation of a digital signal input into a store circuit 701.

[0124] It already asks drawing 31 and the block diagram of concrete 1 example of a circuit is shown in it.

[0125] In this example, the output signal of the silent period detector 3002 is inputted into AND circuit 3103 through a logical negation circuit 3102 in one side. This AND circuit 3103 is a gate circuit which inputs the digital signal from a store circuit 701 into the digital to analog circuit 707, and is made the same configuration as said quantizing-noise clearance circuit 1500. That is, in this example, it is the thing in a silent period from which it already tends to be heard and ** also tends to remove a quantizing noise in the meantime simultaneously.

[0126] The output signal of the above-mentioned silent period detector 3002 is inputted into the control terminal S of a multiplexer 3101. A multiplexer 3101 inputs selectively two clock pulses CK1 and CK2 into an address counter 703 according to the output signal of the silent period detector 3002 inputted into the control terminal S. For example, a clock pulse CK 1 is usually a clock pulse corresponding to playback, and it is made to have a frequency corresponding to the sampling rate of the aforementioned digital signal held. On the other hand, a clock pulse CK 2 is already heard, is used for business, and is made into about about 10 times [of the above-mentioned clock pulse CK 1] high frequency.

[0127] the case where already hear it and the mode is specified -- the silent period detector 3002 -- **** -- an output signal will be set to high level (logic 1) if judged with it being silent. Since the output signal of a logical negation circuit 3102 was set to a low level (logic 0) in response and the gate of AND circuit 3103 was closed, in the

case of the above digital signals of a two's complement code, the digital signal inputted into the digital to analog circuit 707 in a silent period should correspond compulsorily at 0 level. Moreover, with the high level of the output signal of the above-mentioned silent period detector 3002, a multiplexer 3101 is changed into a clock CK 1, and inputs a clock CK 2 into an address counter 703. Thereby, an address counter 703 performs renewal actuation of the address in the usual actuation about 10 times the rate of playback. By this, a silent period is shortened by 10 by about 1/, it is already heard equivalent, and playback is performed.

[0128] According to the experiment of an invention-in-this-application person, the rate that a silent period occupies to the whole playback time amount, such as various conversation and a lecture, also becomes about 30% - 50% from the news program of reading a manuscript, comparatively long. About 2 / 3 - 1/2 can be made to shorten playback time amount by abolishing the silent period of this substantially.

[0129] After the above-mentioned silent period expires, since it returns to usual playback of a basis promptly, tone quality becomes the same with a fundamental tone, and listening comprehension becomes very easy. In addition, what is necessary is just to make the output signal of the silent period detector 3002 input into the control terminal S of a multiplexer 3101 through the newly added AND circuit in this example circuit, when already hearing it and stopping a function. And if 0 is inputted into the input of the above-mentioned AND circuit when not performing ******, since the control terminal S of a multiplexer 3101 is always made into a low level, a clock CK 1 will be inputted into an address counter 703 also in a silent period, and silent level will be outputted only for the time amount corresponding to a silent period. At this time, AND circuit 3103 acts as above quantizing-noise clearance circuits, and prevents generating of a quantizing noise in the meantime.

[0130] The block diagram of concrete 1 example of a ****** circuit is shown in drawing 32 .

[0131] In this example, the silent period expanded in proportion to the true silent period for ****** playback is made. The output signal of the above silent period detectors 3002 is supplied to set input S of a flip-flop circuit 3201 in one side, and is supplied to one input of AND circuit 3210 in another side. The clock pulse CK 3 for measuring a silent period to the input of another side of this AND circuit 3210 is inputted. The output signal of AND circuit 3210 is inputted into the silent period counter 3202. counting corresponding to [while being judged with it being silent by the silent period detector 3002, when the silent period counter 3202 carried out counting of the above-mentioned clock pulse CK 3] the silent time amount -- it operates. counting of the above-mentioned clock pulse CK 3 into which a counter 3205 is inputted through AND circuit 3211 -- it operates. The above-mentioned silent period counter 3202 performs that information maintenance actuation with time amount measurement of the above-mentioned silent period, and rendering actuation of the

above-mentioned silent time amount is performed by the counter 3205 which carries out counting of the same clock pulse CK 3 as this silent hour entry. That is, the output of the above-mentioned silent period counter 3202 and a counter 3205 is inputted into a comparator 3203, and counting of the coincidence output A=B is carried out by the N counter 3204.

[0132] N-ary is made adjustable, although the N counter 3204 is for specifying a silent period N times and it is not restricted especially. The N counter 3204 is a programmable counter, when enumerated data Q are in agreement with N, outputs coincidence signal Q=N and makes the above-mentioned flip-flop circuit 3201 reset. This N counter 3204 is also realizable using a down counter circuit. a borrow when enumerated data perform down count actuation from initial value N and are set to 0 -- it is made to make the above-mentioned flip-flop circuit 3201 reset with an output

[0133] The output signal Q of a flip-flop circuit 3201 is used as a control signal of AND circuit 3208 which is reversed by the logical negation circuit 3209 in one side, and has said quantizing-noise clearance function. And the output signal Q of the above-mentioned flip-flop circuit 3201 is made into the control signal of AND circuit 3206 through control of AND circuit 3211 which supplies a clock pulse CK 3 to the above-mentioned counter 3205, and a logical negation circuit 3207 in another side. This AND circuit 3206 acts on an address counter 703 as a gate circuit which supplies said clock pulse CK 1 selectively.

[0134] The actuation of this example circuit is as follows. If a silent period is detected in the silent period detector 3002, AND circuit 3210 will open the gate and will input a clock pulse CK 3 into the silent period counter 3202. the silent period [while being judged by the silent period detector 3002 as a silent condition and being by this] counter 3202 -- counting of a clock pulse CK 3 -- it operates. If judged with the voice digital signal having been inputted by the silent period detector 3002, a flip-flop circuit 3201 will be set synchronizing with the change to a low level from the high level of the detecting signal. By this, an output signal Q becomes high-level, it replaces with a digital signal from a store circuit 701, and the digital signal corresponding to non-signal level is supplied to the digital to analog circuit 707.

[0135] According to change in the logic 1 of the output signal Q of the above-mentioned flip-flop circuit 3201, the output signal of a logical negation circuit 3207 will become logic 0, and the gate of AND circuit 3206 will be closed. Since a clock pulse CK 1 was not supplied to an address counter 703, an address counter 703 has the front address kept held by this. If it puts in another way, read-out actuation of a store circuit 701 will be stopped. since AND circuit 3211 opens the gate by change in the logic 1 of the output signal Q of the above-mentioned flip-flop circuit 3201 -- a counter 3205 -- counting of a clock pulse CK 3 -- actuation is started. If these enumerated data become equal to the enumerated data of the above-mentioned silent period counter 3202, a comparator 3203 outputs coincidence signal A=B, and a

counter 3205 will be reset while operating the N counter 3204. If the N counter 3204 carries out counting of the N-ary, a flip-flop circuit 3201 will be reset by the repeat of the above actuation. That is, if the silent time amount measured by the above-mentioned silent period counter 3202 N Doubles, a flip-flop circuit 3201 will be reset. By reset of this flip-flop circuit 3201, AND circuit 3206 opens the gate again and inputs a clock pulse CK 1 into an address counter 703. Since the digital signal with which AND circuit 3208 opened the gate and reading appearance was carried out is supplied to the digital to analog circuit 707 while read-out of the substantial digital signal from a store circuit 701 is resumed by this, a sound signal will be outputted again. With this configuration, amplification of a silent period is proportional to the silent period of the fundamental tone of a basis. So, since between conversation or lectures is expanded according to each, it becomes easy to catch.

[0136] In addition, when counting a silent period, the above quantizing noises will be outputted. What is necessary is to reverse the output signal of the silent period detector 3002 through a logical negation circuit, and just to control AND circuit 3208, in order to remove the quantizing noise at the time of the count of this silent period. In this case, while a quantizing noise is removed by the output signal of the silent period detector 3002 where the AND circuit of 3 inputs was used and the addition of AND circuit 3208 was carried out [above-mentioned] at the time of the count of a silent period and the silent period after it is expanded, a quantizing noise is removed by the output signal Q of a flip-flop circuit 3201 as mentioned above.

[0137] Said drawing 31 already asks drawing 33 , and the wave form chart of operation corresponding to a circuit is shown in it. Since the silent period 3303 (Tm1) of the HARASHIN number 3301 and 3304 (Tm2) can switch the clock pulse to which the meantime is supplied by the address counter 703 and can delete substantially, if it puts in another way, without changing the pitch (frequency) of a sound signal, ****** will become possible, without degrading the tone quality of a sound signal.

[0138] The wave form chart of operation corresponding to the ****** circuit of said drawing 32 is shown in drawing 34 . Since actuation of the address counter 703 in the meantime is suspended by the counter 3205 and the N counter 3204 and the silent period 3303 (Tm1) of the HARASHIN number 3301 and 3304 (Tm2) are expanded by n times, respectively, if it puts in another way, without changing the pitch (frequency) of a sound signal, ****** will become possible, without degrading the tone quality of a sound signal.

[0139] this invention is started at drawing 35 -- it is already heard and the block diagram of other one example of a circuit is shown.

[0140] In this example, it is already heard, and for playback, an adder circuit 3501 is used for an address counter 3503, and the address-generation actuation itself is switched. That is, an address counter 3503 is inputted into a multiplexer 702 as the read-out address of a store circuit 701 while it consists of a register 3502 which

receives an adder circuit 3501 and its addition output A+B and the output signal Q of a register 3502 returns to the addition input A.

[0141] 1 and positive integer M are selectively inputted through a multiplexer 3504 in the input B of another side of an adder circuit 3501. The output signal of the silent period detector 3002 is supplied to the control terminal S of this multiplexer 3504. The output signal of the silent period detector 3002 is supplied also to AND circuit 3505 which performs quantizing-noise clearance through a logical negation circuit 3209 like said example.

[0142] If judged with a silent period by the silent period detector 3002, a multiplexer 3504 will be replaced with 1, will choose M, and will tell it to an adder circuit 3501. Therefore, before entering at a silent period, an adder circuit 3501 performs count actuation of +1 of adding +1 to the address signal formed with the register 3502, and generating the following address signal. On the other hand, if it enters with a silent period as mentioned above, a multiplexer 3504 will input M into an adder circuit 3501. Consequently, an adder circuit 3501 adds +M to the address signal formed with the register 3502, and generates the address signal made to skip by M address. Thereby, the renewal actuation of the address in a silent period becomes a high speed equivalent, and substantial deletion of a silent period is performed to said this appearance.

[0143] The block diagram of other concrete 1 examples of the ****** circuit concerning this invention is shown in drawing 36 .

[0144] In this example, the clock pulse CK 4 for ****** is prepared for ****** playback. that is, it was shown in said drawing 31 -- it is already heard, and with a circuit, if the late clock pulse CK 4 is prepared for ****** and it goes into reverse at a silent period, a multiplexer 3601 will be switched to it and it will switch to it from the usual clock pulse CK 1 at the clock pulse CK 4 for ******. If it is made low to the above-mentioned clock pulse CK 1 at 1-/N of the frequency of a clock pulse CK 4, actuation of an address counter 703 increases slow N times, and a silent period can be expanded by N times equivalent.

[0145] Since the same circuit as said drawing 31 can constitute from this example, if it is already heard through the same multiplexer or a suitable switch circuit to the input B of a multiplexer 3601, and a clock pulse CK 2 is supplied at the time of the mode and a clock pulse CK 4 is selectively supplied, respectively at the time of ****** mode, ****** and ****** playback will be attained.

[0146] The block diagram of other one concrete example of the ****** circuit concerning this invention is shown in drawing 37 .

[0147] In ****** mode, convenience of listening comprehension in case a user is an old man etc. as mentioned above is carried out. therefore, it is actually made hard to catch when amplification and extension of the period are performed also to a comparatively long silent period -- things -- ** So, in this example, the function to

prepare a fixed limit is added to amplification thru/or extension of a silent period with ****** mode.

[0148] The following circuits are added on the basis of the ****** circuit which showed this example to said drawing 32 . The output signal Q of the silent period counter 3202 is supplied to the multiplication circuit 3703, and it increases it N times. The multiplication output which it increased these N times is supplied to one input A of a multiplexer 3705, and one input A of a comparator 3706. The output signal Q of the above-mentioned silent period counter 3202 is supplied to one input A of a comparator 3707. The maximum extension time amount K of a silent period is inputted into the input of another side of the above-mentioned multiplexer 3705 and two comparators 3706 and 3707. Although neither the N-ary which increases the above-mentioned silent period N times, nor especially the maximum extension time amount K is restricted, it enables it to be set as arbitration in the fixed range in the user of a player. Although not restricted especially, adjustment of the maximum extension time amount K is enabled in the range for 1 - 5 seconds. In the result of the ****** audition by an invention-in-this-application person etc., it judged that about 3 seconds is suitable.

[0149] The output signal Q of the counter 3702 for extension is supplied to one input A of a comparator 3704, and the output signal Y of the above-mentioned multiplexer 3705 is supplied to the input B of another side. The output signal of a comparator 3706 is supplied to the control terminal S of the above-mentioned multiplexer 3705. And the output signal of comparators 3704 and 3707 is supplied to the reset terminal R of a flip-flop circuit 3714, the reset terminal R of the silent period counter 3202, and the reset terminal R of the counter 3702 for extension through OR circuit G4. If the silent period detector 3002 falls to said this appearance and the above-mentioned flip-flop circuit 3714 is put in another way as it, it will be set to the termination timing of the silent period of the HARASHIN number 3301. the output signal Q of this flip-flop circuit 3714 -- a logical negation circuit 3713 -- minding -- control of above AND circuits 3712 and counting of the counter 3702 for extension -- AND circuit 3711 and logical negation circuit 3709 which control actuation -- minding -- counting of an address counter 703 -- AND circuit 3708 which controls actuation is supplied.

[0150] The conceptual diagram of operation for explaining an example of actuation of drawing 37 is shown in drawing 38 . It is the HARASHIN number 3801 before processing, and Tmax is equivalent to the maximum extension time amount K. Thus, if the output signal Q of the silent period counter 3202 with which it is supplied to the input A of a comparator 3707 when the silent period Td of the HARASHIN number 3801 before processing is larger than the above-mentioned maximum extension time amount K becomes larger than the maximum extension time amount K supplied to the input B of a comparator 3707, comparison output A>=B of a comparator 3707 will become logic 1. Thereby, since a flip-flop circuit 3714, the silent period counter 3202,

and the counter 3702 for extension are reset through OR circuit 3701, ****** mode is made into an invalid equivalent. This becomes the same a ****** actuation processing front and after processing. Thus, when long, extended actuation of a silent period is substantially made into an invalid, so that the silent period in the HARASHIN number 3801 may exceed the object of ******.

[0151] The conceptual diagram of operation for explaining other examples of actuation of drawing 37 is shown in drawing 39 . Also in this drawing, it is the HARASHIN number 3901 before processing like the above, and Tmax is equivalent to the maximum extension time amount K. Thus, although the silent period Td of the HARASHIN number 3901 before processing is shorter than the above-mentioned maximum extension time amount K, if it N Doubles, when becoming longer than the maximum extension time amount K, a comparator 3706 detects that silent time amount TdxN calculated by the multiplication circuit 3703 becomes larger than the maximum extension time amount K, and it makes the comparison output A>=B logic 1. According to the logic 1 of this comparison output signal, a multiplexer 3705 is replaced with multiplication output TdxN of Input A, and tells the maximum extension time amount K of Input B to a comparator 3704. Thereby, if the output signal Q of the counter 3702 for extension exceeds the above-mentioned maximum extension time delay, comparison output A>=B of a comparator 3704 will become logic 1, and will reset a flip-flop circuit 3714, the silent period counter 3202, and the counter 3702 for extension through OR circuit 3701. Thus, it is restricted so that the extended time amount of a silent period may not exceed the above-mentioned maximum extension time amount in the signal 3902 after processing.

[0152] The conceptual diagram of operation for explaining an example of further others of actuation of drawing 37 is shown in drawing 40 . Also in this drawing, it is the HARASHIN number 4001 before processing like the above, and Tmax is equivalent to the maximum extension time amount K. Thus, the silent period Td of the HARASHIN number 4001 before processing is shorter than the above-mentioned maximum extension time amount K, and when what doubled it N becomes shorter than the maximum extension time amount K, a comparator 3706 detects that silent time amount TdxN calculated by the multiplication circuit 3703 becomes smaller than the maximum extension time amount K, and the comparison output A>=B is made into logic 0. According to the logic 0 of this comparison output signal, a multiplexer 3705 tells multiplication output TdxN of Input A to a comparator 3704. If the output signal Q of the counter 3702 for extension exceeds by this silent period TdxN by which amplification was carried out [above-mentioned], comparison output A>=B of a comparator 3704 will become logic 1, and will reset a flip-flop circuit 3714, the silent period counter 3202, and the counter 3702 for extension through OR circuit 3701. Thus, in the signal 4002 after processing, the silent period was expanded by N times.

[0153] The wave form chart for explaining other one example of ****** and ******

actuation is shown in drawing 41 .

[0154] In this example, it is already heard and is made to perform a data compression function besides ********. Conversely, if it says, the silent periods 3303 and 3304 of the HARASHIN number 3301 will be transposed to the non-corresponded number 4102 (MK) like the processing signal 4101. In addition, the non-corresponded number 4102 of this drawing (MK) shows the insertion point, and when analogue conversion is carried out actually, it changes into a silent condition the part in which the non-corresponded number 4102 (MK) was inserted. Since it is transposed to information [as / whose silent periods 3303 and 3304 are several bytes by making such a non-corresponded number 4102 (MK) insert], the silent periods 3303 and 3304 included in the digital signal before analogue conversion is carried out can be abolished substantially. Consequently, about about 1 / two to 2/3 are decreased as mentioned above by the rate which a silent period [as opposed to the whole in storage capacity required for storage of a digital signal] occupies, and things are made. making it expand selectively by using the above-mentioned silent signal 4102 (MK), when such a data compression approach is adopted, or making it reduce -- ****** -- it can be made to operate by already hearing it fundamentally above to such a data compression -- it can already be heard and a circuit can be used. What is necessary is replacing with it and making it just make the non-corresponded number 4102 (MK) insert, although it was made to make 0 level output in order to already hear it and to remove the quantizing noise of a silent period in a circuit.

[0155] Bit pattern drawing of one example of the non-corresponded number 4102 (MK) is shown in drawing 42 .

[0156] The non-corresponded number 4102 (MK) consists of a silent mark 4203 and silent period information 4204. The combination of the bit pattern which the silent mark 4203 is the usual voice digital signal, and is not obtained is chosen. In this example, when a digital signal consists of a two's complement code, the combination of the forward maximum 4201 (01111111) and the negative maximum 4202 (1 million) is used. Since it does not change from forward maximum to negative maximum as a usual sound signal, this combination is used as a silent mark. As the above-mentioned silent mark 4203, you may constitute combining 3 bytes besides the combination of reverse, or 2 bytes, or 4 bytes with the above-mentioned case.

[0157] Especially the silent period information 4204 is prepared by 2 bytes, although not restricted. In order to make it correspond also to a silent period longer than this, 3 bytes, 4 etc. bytes, etc. may be used for the silent period information 4204.

[0158] The block diagram of one example of the digital signal regenerative circuit which already hears it and contains /****** mode to the digital signal with which the above data compressions were performed is shown in drawing 43 .

[0159] The clock ADCK for address counters is supplied to an address counter 703 through AND circuit 4311. The read-out signal of a store circuit 701 is outputted

through four steps of shift registers 4301a–4301d corresponding to it, when the non–corresponded number 4102 (MK) consists of the silent mark 4203 and 2 bytes of silent time amount which are 2 bytes as mentioned above. As for these shift registers 4301a–4301d, the data shift clock DSCK is supplied through AND circuit 4312. The outputs A and B of the above–mentioned shift registers 4301d and 4301c are inputted into the mark detection circuit 4303. The mark detection circuit 4303 performs a comparison test in accordance with the maximum 4202 (1 million) said forward maximum 4201 (01111111) and negative in the bit pattern of the above–mentioned signals A and B. The detecting signal of the mark detection circuit 4303 is used as a set signal of flip–flops 4308 and 4309. The outputs C and D of shift registers 4301b and 4301a are supplied to one input A of a comparator 4304. The output signal of the silent counter 4305 is supplied to the input B of another side of this comparator 4304. The output signal of the above–mentioned comparator 4304 is supplied to the input CK of the loop counter 4306 used for the reset terminal R of the silent counter 4305, and extension of a silent period through OR circuit 4315. The output Q of this loop counter 4306 is compared with the extended scale factor N by the comparator 4307.

[0160] The output Q of a flip–flop circuit 4309 is supplied to above–mentioned OR circuit 4315 and AND circuits 4311 and 4312 through a logical negation circuit 4314. Thereby, if the silent mark 4203 is detected, actuation of an address counter 703 and a shift registers [4301a–4301d] shift action will be stopped, and the non–corresponded number 4102 (MK) will be held at shift registers 4301a–4301d. At this time, a store circuit 701 is also made into a read–out idle state according to a halt of an address counter 703 of operation. The output signal of the above–mentioned comparator 4307 is supplied to the reset terminal R of the loop counter 4306 and a flip–flop circuit 4309.

[0161] The output Q of a flip–flop circuit 4308 is made into the silent flag FLG, and is made into the control signal of AND circuit 4310 through a logical negation circuit 4313. Thus, detection of the silent mark 4203 prevents that AND circuit 4310 will be closed promptly and maximum 4201, the forward negative maximum 4202, and the forward hour entry 4204 continued and outputted will be accidentally outputted as a sound signal. In using forward and negative maximum as a silent mark 4203 as mentioned above especially, if it is outputted as it is, the noise of big pulse nature will occur.

[0162] The silent flag of the above–mentioned flip–flop circuit 4308 returns as a reset signal of a flip–flop circuit 4308 through four steps of D type flip–flops 4302a–4302d. These flip–flop circuits 4302a–4302d perform transfer actuation of a silent flag with the same data shift clock as said shift registers 4301a–4301d so that it may explain below, and they detect the period when the non–corresponded number 4102 (MK) which consists of the above silent marks 4203 currently held with termination of a silent period at the above–mentioned shift registers 4301a–4301d and a hour entry

4204 is swept out. If judged with the non-corresponded number period having expired by these flip-flop circuits 4302a-4302d, reset of a flip-flop circuit 4308 will be performed.

[0163] A set of a flip-flop circuit 4309 of detection of the silent mark 4203 cancels the reset condition of the silent counter 4305 through a logical negation circuit 4314. the silent counter 4305 -- discharge of this reset condition -- responding -- counting of the silent clock SCLK -- actuation is started.

[0164] At the time of the usual playback mode, the N-ary supplied to a comparator 4307 is set as 1. If the enumerated data of the silent counter 4305 and the silent time amount 4204 included in the non-corresponded number 4102 (MK) are in agreement by this, since the loop counter 4306 carries out counting of +1, enumerated data will be set to 1 in the coincidence signal outputted by the comparator 4304. Consequently, since a comparator 4307 also forms a coincidence output simultaneously, reset of the loop counter 4306 and a flip-flop circuit 4309 is performed. Read-out of the store circuit 701 where AND circuits 4311 and 4312 opened the gate, and minded the address counter 703 by reset of a flip-flop circuit 4309, and a shift registers [4301a-4301d] shift action are resumed. Synchronizing with actuation of these shift registers 4301a-4301d, flip-flop circuits 4302a-4302d also carry out the sequential transfer of the silent flag FLG. That is, it forbids a flip-flop circuit 4308 being told to it by the digital to analog circuit 707 as with a set condition, and being outputted as a voice noise until the non-corresponded number 4102 (MK) currently held at shift registers 4301a-4301d is swept out. A flip-flop circuit 4308 is reset synchronizing with the above-mentioned silent signal 4102 (MK) being swept out. The digital sound signal which a substantial silent period expires by this and is outputted from shift register 4301d of the last stage is inputted into the digital to analog circuit 707 through AND circuit 4310, and playback of a sound signal is performed.

[0165] At the time of ****** mode, the N-ary supplied to a comparator 4307 is set as one or more suitable integral values. For example, when were set as 2 and the enumerated data of the silent counter 4305 and the silent time amount included in the non-corresponded number 4102 (MK) take the 2 surroundings, the silent period when the comparator 4307 formed the coincidence output at and was extended twice is terminated. If Above N is set as 3, the amplification extension of the silent period can be made to increase 3 times of the original silent time amount.

[0166] already -- hearing it -- the mode -- coming -- being alike -- actuation of a flip-flop circuit 4309 is made into an invalid. What is necessary is making it just specifically forbid that the output signal of the mark detection circuit 4303 is supplied to set input S of a flip-flop circuit 4309 through an AND circuit etc. In this case, since a clock is succeedingly supplied to an address counter 703 or shift registers 4301a-4301d, read-out actuation of a store circuit 701 is performed continuously. However, since a flip-flop circuit 4308 is set by the detection output of the mark

detection circuit 4303, it is forbidden with a logical negation circuit 4313 and AND circuit 4310 that the above-mentioned silent signal 4102 (MK) should be inputted into the digital to analog circuit 707 as a sound signal. namely, **** to which a silent period outputs the above-mentioned speech information -- only a short period comes and silent time amount can be abolished substantially. Consequently, said same ****** can be performed.

[0167] The digital-signal-processing circuit which more than already hears it and/or realizes ****** mode can be widely used for various regenerative apparatus including the digital-signal-processing circuit which carries out analog voice playback of the digital sound signal like a digital audio tape (DAT) besides what is used for the player in the above digital signal delivery systems.

[0168] In a digital audio, in order to lengthen sound recording time amount, compression-ization of a sign is performed. and an ecad PCM like [the well-known compression method in which this application presentation carries out digital signal delivery and which can be adopted also in a system] the following explanation and an ecad -- difference -- there are PCM, ecad deltaM, etc. In this, an ecad difference PCM system is adopted as speech compression methods, such as CD-I and CD-ROM, and is standardized as a standard. In addition, what is necessary is just to adopt as data compression-ization the thing suitable for the object and configuration of systems, such as a compression-ized method, and a data compression, an expanding method various [containing the three above-mentioned methods] by this invention mentioned later, and standardizing is desirable.

[0169] Although the amplitude of an acoustic signal and frequency distribution are comparatively quiet with time amount, they change substantially. Then, there is an ecad PCM (APCM) as coding to which a quantization step size is changed according to the property of a nearby signal. In this ecad PCM, a quantization step size is changed according to the amplitude of the quantization value of the last sample. moreover, an ecad -- difference -- PCM -- difference -- an ecad step size is introduced into PCM, and direct quantization of a signal is not carried out, but application quantization of the difference with a forecast is carried out. And deltaM is the coding approach which quantizes a signal by 1 bit. As for this approach, distortion will become large if a signal changes rapidly. On the other hand, ecad deltaM increases a quantization step size, when the same sign continues, and when reversed, it is made small.

[0170] on the other hand, the above-mentioned ecad PCM and an ecad -- difference -- in PCM and ecad deltaM, the multiplication circuit for all changing a step size is needed, the complicated circuit like a microcomputer or a digital signal processor is needed, and there is a fault that circuit magnitude becomes large. Moreover, in deltaM, there is a fault that quantization distortion lacks in fidelity greatly.

[0171] It is suitable for a miniaturization with the easy configuration concerning this

invention, and the block diagram of the example about the advantageous data compression also in power and an expanding method is shown in drawing 44 , drawing 45 , and drawing 46 .

[0172] The object of this example is to offer the data-conversion method from which high fidelity is obtained by the easy configuration about a data compression and expanding, and a data-conversion circuit.

[0173] The block diagram of one example of the data-conversion circuit constituted by the data-conversion method concerning this invention is shown in drawing 44 .

[0174] Although not restricted especially, the data-conversion circuit of this example is turned to the circuit which makes it compress and output to the digital data which consists of 8 bits while transforming an analog signal to the digital data which consists of 16 bits.

[0175] An analog signal Vin is inputted into an analog / digital conversion circuit 4401, and is changed into the digital data which consists of n bits (for example, as mentioned above 16 bits) here. In this example, in order to make the 16-bit data by which digital conversion was carried out [above-mentioned] compress into the data of m (for example, 8 bits), the following circuits are used.

[0176] The 16-bit data D1 by which digital conversion was carried out [above-mentioned] at one input of a subtractor 4402 are inputted. The 16-bit data D2 memorized by the input of another side of a subtractor 4402 at the register 4406 are inputted. Let the 16-bit data D2 memorized by this register 4406 be sampling data in front of one so that it may mention later. A subtractor 4402 subtracts the sampling data D2 before [one] being made to memorize from the input data D1 by which digital conversion was carried out [above-mentioned] by the register 4406, and makes the data D3 of the difference (D1-D2) output. The data D3 of this difference are supplied to one input B of a comparator 4403. The data D4 corresponding to the maximum of the 8-bit data compressed are supplied to the input A of another side of a comparator 4403. This data D4 consists of 16 bits of 0000000011111111, as shown in this drawing, and 8 bits (m) of low order are data (it is 255 at decimal system) of 1 altogether.

[0177] A comparator 4403 performs the size comparison of the data D3 and D4 supplied to input terminals A and B, forms a high-level output signal at the time of B>A (D3> D4), and if it is A>B, it forms the output signal of a low level. The output signal of this comparator 4403 is used as a selector selection signal.

[0178] the maximum data d4 (11111111) which become one input A of a selector 4404 from the above-mentioned 8 bits by which compression is carried out input -- having -- **** -- Input B -- the above -- the data d3 for 8 bits of low order of the data D3 of difference are inputted. If this selector 4404 has the high-level output signal of the above-mentioned comparator 4403 and it puts in another way, when the above-mentioned subtraction data D3 are larger than D4 When the above-mentioned subtraction data D3 are smaller than D4, the data d3 of 8 bits of low order of the

subtraction output supplied to Input B are made to output, if the maximum data d4 of Input A are made to choose and output, and the output signal of the above-mentioned comparator 4403 is a low level and it puts in another way.

[0179] Although especially the output signal d5 of the above-mentioned selector 4404 is not restricted, a store circuit 4408 is made to once memorize it, and it is made to output it as 8-bit digital data Dout read and compressed. The output signal d5 of the above-mentioned selector 4404 is supplied to one input of an adder 4405. The output data D2 of the above-mentioned register 4406 are supplied to the input of another side of this adder 4405. Thereby, an adder 4405 adds the compressed data d5 which were outputted to the sampling data D2 before [one] the register 4406 memorized from above-mentioned SERETAKU, forms updated sampling-data D2' which is made into one before to the data D1 inputted into a degree, and is stored in a register 4406. Thus, an accumulated error can be made to prevent by making the following sampling data generate with a register 4406 and an adder 4405.

[0180] It changes into the data d5 which compressed the 16 bits (n bits) input data D1 into 8 bits (m bits) by the same repeat as the above hereafter.

[0181] The wave form chart for explaining the analog / digital conversion actuation accompanied by the above-mentioned data compression actuation is shown in drawing 45 .

[0182] The data of a register 4406 are cleared at the time of data compression initiation (0000000000000000). Therefore, if an analog signal takes action on rapid decrease as shown in this drawing, in progressive addition actuation of the maximum of 8 bits of low order, it cannot follow to an input digital signal, but once the difference of an input digital signal and the sampling data in front of one becomes below the maximum of the above-mentioned compressed data, the compressed data which corresponded to change of an input signal faithfully can be obtained. in an acoustic signal, with time amount, it comes out and, as for the amplitude and frequency distribution, data compression-ization with the comparatively quiet fidelity which is satisfactory practically is attained.

[0183] The block diagram of other one example of the data-conversion circuit by the data-conversion method concerning this invention is shown in drawing 46 . In this example, while making n bits (16 bits) data elongate the data which you were made to compress into m bits (8 bit of for example, **) corresponding to said example, it is turned to the circuit made to change and output to an analog signal.

[0184] Although especially the data Din compressed by data compression circuit like said drawing 44 are not restricted, from the store circuit 4408 of drawing 44 , it is transmitted to the store circuit 4601 of drawing 46 , and they are once memorized. Depending on the case, the store circuit 4408 of drawing 44 and the store circuit 4601 of drawing 46 are used in common. The data d5 by which reading appearance was carried out from this store circuit 4601 are supplied to one input of an adder 4602.

The n-bit data D6 memorized by the register 4603 are supplied to the input of another side of an adder 4602. The above-mentioned data d5 add data D6, and an adder 4602 forms data D7. Although especially this data D7 is not restricted, let it be input data of a register 4603. And as data by which the data D6 outputted from that of the above-mentioned register 4603 were expanded, it inputs into the digital to analog circuit 4604, and analog signal Vout to which it restored is formed in it.

[0185] The actuation of a data growth long-gyrus-of-insula way is as follows. A register 4603 is cleared by said this appearance at the time of data decompression actuation initiation. The compressed data d5 by which reading appearance was carried out from the store circuit 4601 is added with the data D6 of the register 4603 which consists of n bits in front of one for every read-out, and is memorized by the register 4603 as elongated data. Therefore, the expanding data which change stair-like according to a changed part by compressed data d5 like drawing 45 can be restored.

[0186] The operation effectiveness acquired from the above this example is as follows. Namely, (1) It asks for difference with the data inputted as the sampling data in front of one, in being larger than the maximum of the sign into which difference is compressed, it outputs maximum, and the data which were made to output a subtraction result and were compressed when small are outputted, and a data compression is performed. By this method, the effectiveness that on comparatively quiet data and easy configurations [distribution / the amplitude or / frequency / time amount], such as subtraction and addition, can perform a data compression with high fidelity is acquired like an acoustic signal.

[0187] (2) The effectiveness that a data compression and an expanding circuit can be realized by easy circuits, such as a subtractor, an adder, a register, and a comparator, and can also stop the power consumption small by the above (1) is acquired.

[0188] (3) By using the above data-conversion methods and circuits, the effectiveness that small lightweight-ization of the player which reproduces the acoustic signal memorized in the store circuit is realizable is acquired.

[0189] Although invention made from this invention person above was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which the invention in this application is not limited to said example, and does not deviate from the summary. For example, in drawing 44 , it may replace with the configuration which compares the maximum D4 of the subtraction output data D3 and the data compressed with a comparator, and at least 1 bit of the high order bit of the subtraction output data D3 may form a size comparison output with the above-mentioned maximum equivalent with being 1 using an OR circuit etc. The data of difference may use the thing which made the input data D1 subtract from the data D2 of a register.

[0190] It cannot be overemphasized that the data with which digital conversion of the thing using the output signal of an analog / digital conversion circuit like the example

of drawing 44 in the input signal by which a data compression is carried out others was carried out may be memorized by a ****** store circuit, a magnetic tape, or the compact disk. The compressed data are changed into serial data and it is made to make them output through a communication line etc.

[0191] The data-conversion method and data-conversion circuit concerning this invention can be widely used for the circuit and equipment treating the digital data which changes with the passage of time.

[0192] The block diagram of one example of the digital to analog circuit concerning this invention is shown in drawing 47 . Although especially the digital to analog circuit of this drawing is not restricted, it is carried in the player 101 used for said digital signal delivery system.

[0193] There is said official report (JP,61-236222,A) as a well-known technique of a digital to analog circuit. In this digital to analog circuit, the pulse of a predetermined frequency is repeated with a counter, and carries out counting, the output signal of this counter is compared with the input digital signal which should be changed in digital one, the pulse which has the width of face corresponding to the value of an input digital signal is outputted, a filter circuit removes a high frequency component from a pulse output, and an analog signal is formed.

[0194] In the above-mentioned digital to analog circuit, since it is what forms the output signal changed into one pulse width to the input digital signal, there is a problem that smoothness, then a ripple component generate it in a filter circuit, and the good analog signal of tone quality is not acquired. That is, in order to improve responsibility (high region property) of an analog signal, it is necessary to make the time constant of a low pass filter small but, and if it does in this way, said ripple component will increase. If the time constant of a filter circuit is enlarged in order to lessen this ripple component, the responsibility over input signal change will worsen and a high region property will deteriorate. Moreover, since it is what needs a counter and a comparator, circuitry becomes complicated.

[0195] The digital to analog circuit of drawing 47 is turned to the improvement of the above-mentioned output characteristics.

[0196] Digital to analog circuits of this example are consisted of by the following circuits in order to remove the ripple component contained in an output signal. The input digital signal Din is incorporated by the register 4701. The input digital signal Din with which this register 4701 was incorporated is supplied to one input A of a comparator 4702. A counter 4703 performs actuation which repeats and carries out counting of the pulse as a conventional-time signal. The carry output CAR of this counter 4703 is supplied to a repeat counter 4704. A repeat counter 4704 will output the carry output CAR, if counting of the specified repeat enumerated data J is carried out. This carry output CAR is inputted into a control circuit 4705, and the conversion terminate signal EOC is outputted here.

[0197] If the strobe which synchronized with the input digital signal Din is received, a control circuit 4705 supplies the set signal S to a register 4701, and directs incorporation of the input digital signal Din. moreover -- although not restricted especially, if the input digital signal Din to the above-mentioned register 4701 is incorporated in response to the 10MHz conventional-time pulse CK -- it -- a counter 4703 -- supplying -- counting -- actuation is made to start

[0198] A comparator 4702 forms a high-level output signal at the time when the input digital signal Din incorporated by the register 4701 is larger than enumerated data Q to a counter 4703 (A>B). and the data-line input digital signal Din -- receiving -- counting of a counter 4703 -- if an output Q becomes large (A<B), the output signal of a low level will be formed. in this example, since the repeat counter 4704 was formed, the output pulse corresponding to the following input digital signal was not promptly formed like before, but the pulse with the pulse width corresponding to the one above-mentioned input digital signal Din was specified by the repeat counter 4704 -- conversion actuation is ended repeatedly J times.

[0199] The wave form chart of an example of actuation of the above-mentioned digital to analog circuit is shown in drawing 48 .

[0200] For example, when a digital input signal Din consists of 8 bits, the period of the circumference of one is set to 25.6 microseconds as mentioned above by carrying out counting using the counter which the period of the 10MHz clock pulse CK is set to 0.1 microseconds, and consists of 8 bits. Therefore, when an input digital signal is 1 of decimal system, for 0.1 microseconds of the beginning is high-level, and the pulse of a low level is outputted for for remaining 25.5 microseconds. Moreover, when an input digital signal is a decimal 10, for 1 microsecond of the beginning is high-level, and the pulse of a low level is outputted for for remaining 24.6 microseconds. Similarly, when an input digital signal is 100 of decimal system, for 10 microseconds of the beginning is high-level, and the pulse of a low level is outputted for for remaining 15.6 microseconds. And when an input digital signal is 255 which is the maximum of decimal system, it is high-level for 25.5 microseconds of the beginning, and the pulse of a low level is outputted only for remaining 0.1 microseconds.

[0201] The case where the count J of a repeat is 4 is shown in this drawing. If the output signal changed into the above pulse width is outputted repeatedly 4 times, the conversion output signal EOC corresponding to one input digital signal Din will be outputted. Thus, if four repeats are performed, in 1 sampling period and the aforementioned player 101, in order to form four above-mentioned Pulse-Density-Modulation outputs in the period which fetches the data by which reading appearance was carried out from the store circuit 701, 25.6x4=102.4microsecond will come as a conversion time, and the conversion frequency of about 10kHz will become possible. This becomes the optimal thing for playback of a news program, conversation, a lecture, etc., etc. In playback of the music

program of the quality of loud sound, if the frequency of the above-mentioned clock pulse CK is set to 20MHz, the high region frequency to about 20kHz under 4 times of the same counts of a repeat is reproducible. Moreover, if the number of repeats is reduced for the above-mentioned clock pulse CK to 2 times as with 10Mz(es), the high region frequency to 20kHz is reproducible similarly. Thus, what is necessary is for the frequency of the above-mentioned clock pulse CK and the count of a repeat to combine, and just to make it double with the sampling period of an input digital signal.

[0202] In addition, if a digital signal is again inputted in response to the above-mentioned conversion output signal EOC synchronizing with Strobe STB, the analog / digital conversion actuation corresponding to it will be performed similarly.

[0203] Smoothness is carried out with the low pass filter 4708 which consists of resistance 4706 and a capacitor 4707, and the Pulse-Density-Modulation signal outputted from the above-mentioned comparator 4702 is analog signal Dout. It is outputted. In this example, two or more pulses by which Pulse Density Modulation was carried out as mentioned above are outputted. Therefore, even if it sets up the time constant of resistance 4706 and a capacitor 4707 small and makes responsibility high for quality[of loud sound]-izing of an output signal, a ripple component can be prevented to min.

[0204] In the circuit shown in this example, since the whole circuit can constitute by the digital circuit, compared with the case where a digital circuit and an analog circuit are made intermingled, a process is easy and can form with the CMOS-circuit integrated circuit of a low power etc.

[0205] The block diagram of other one example of the digital to analog circuit concerning this invention is shown in drawing 49 . The digital to analog circuit of this example is turned to the simplification of a circuit.

[0206] In this example, the comparator 4702 of drawing 47 is omitted and the Pulse-Density-Modulation signal corresponding to a digital signal is formed by the down counter 4901 and the flip-flop circuit 4902. That is, the input digital signal Din is set to the down counter 4901 synchronizing with a strobe. Moreover, a flip-flop circuit 4902 is set by the above-mentioned strobe. thereby -- the output signal Q of a flip-flop circuit 4902 -- high-level -- changing -- the above-mentioned strobe -- the down counter 4901 -- counting of a clock -- actuation is started. if, as for the down counter 4901, enumerated data are set to 0 -- a borrow -- Signal BO is outputted and the above-mentioned flip-flop circuit 4902 is made to reset this borrow -- Signal BO is sent to an input side as a conversion terminate signal.

[0207] a flip-flop circuit 4902 -- counting of a digital signal -- it is set with initiation, and it will be reset if counting of the clock corresponding to the digital signal is carried out. Thereby, the output signal Q of a flip-flop circuit 4902 is made into the Pulse-Density-Modulation signal corresponding to an input digital signal.

[0208] The source of a signal established in the input side of the digital to analog

circuit of this example outputs a digital signal and a strobe like said store circuit 701 corresponding to a fixed sampling period. therefore, the thing for which the above-mentioned conversion terminate signal EOC was sent in the source side of a signal -- having -- promptly -- the following digital signal -- not sending out -- that -- as one condition -- up Norikazu -- a digital signal and a strobe are sent out synchronizing with the sampling period of a law. the set actuation which synchronized with the strobe of a flip-flop circuit 4902 by this, and the borrow of the down counter 4901 -- the Pulse-Density-Modulation signal corresponding to the input digital signal of a fixed period can be acquired by the reset action which synchronized with the output BO.

[0209] For example, when a digital input signal Din consists of 8 bits, if the 10MHz clock pulse CK is used as mentioned above, the maximum enumerated data will be set to 25.5 microseconds by carrying out counting of it for ** using the down counter 4901 which the period is set to 0.1 microseconds and consists of 8 bits. Therefore, when an input digital signal is 1 of decimal system, the pulse of a low level is outputted for for remaining 25.5 microseconds until for 0.1 microseconds of the beginning is high-level since the down counter 4901 carries out counting only of 1, and the following strobe is inputted. Moreover, when an input digital signal is a decimal 10, the pulse of a low level is outputted for for remaining 24.6 microseconds until for 1 microsecond of the beginning while carrying out counting of 10 is high-level and the following strobe is inputted. Similarly, when an input digital signal is 100 of decimal system, the pulse of a low level is outputted for for remaining 15.6 microseconds until for 10 microseconds while carrying out counting of 100 is high-level and the following strobe is inputted. And when an input digital signal is 255 which is the maximum of decimal system, it is high-level for 25.5 microseconds corresponding to the maximum enumerated data, and remains, and the pulse of a low level is outputted only for 0.1 microseconds.

[0210] Smoothness is carried out to the above resistance 4903 with a low pass filter 4905 like a capacitor 4904, and such a Pulse-Density-Modulation signal is analog signal Vout. It is formed.

[0211] In addition, what is necessary is just to carry out multiple-times generating of the strobe of the aforementioned period to one input signal Din by the input side, in forming two or more Pulse-Density-Modulation signals to one input signal Din like the example of drawing 47 drawing.

[0212] The block diagram of one example of further others of the digital to analog circuit concerning this invention is shown in drawing 50 .

[0213] It will be necessary to form a digital signal and a strobe a fixed period in an input side, and the application will be restricted in the digital to analog circuit shown in said drawing 49 . This example prescribes the period of the Pulse-Density-Modulation signal outputted by forming the rise counter 5002. That is, 0 is supplied to the input D

of the rise counter 5002, and while being cleared by the counter load pulse LD which synchronized with the strobe, in the down counter 5001, the input digital signal Din is incorporated by the above-mentioned counter load pulse LD.

[0214] The same clock CK is supplied to the above-mentioned down counter 5001 and the rise counter 5002. the borrow of the down counter 5001 -- an output BO is supplied to one input of AND circuit 5006 through Input K and the logical negation circuit 5005 of a flip-flop circuit 5003. The above-mentioned clock pulse is supplied to the clock terminal CK of a flip-flop circuit 5003, and the output signal of AND circuit 5006 is supplied to the input J of a flip-flop circuit 5003. The set signal generated from the control circuit 5004 is supplied to the input of another side of this AND circuit 5006. And the carry output CAR of the above-mentioned counter is supplied to a control circuit 5004.

[0215] If the strobe ST inputted synchronizing with a digital signal Din is received, a control circuit 5004 will be made into operating state, and will output the counter load signal LD of the above-mentioned down counter 5001 and the rise counter 5002, and the set signal FR of a flip-flop circuit 5003. Moreover, a control circuit 5004 will send out a clock pulse to the down counter 5001 and rise counter 5002 grade, if a strobe is inputted in response to Clock CLK, if the KIRYA output CAR from the rise counter 5002 is undergone, sends out the conversion terminate signal EOC and will be in a standby condition.

[0216] A flip-flop circuit 5003 operates synchronizing with the rising edge of a clock pulse, if they are inputs J and K00 (a low level, low level) then, it will be in a maintenance condition, if it is inputs J and K01 (a low level, high level), it will be in a reset condition, if it is inputs J and K10 (high level, low level), it will be in a set condition, and reversal actuation is performed if it is inputs J and K11 (high level, high level).

[0217] Next, the above-mentioned digital to analog actuation is explained to a detail.

[0218] In an initial state, all counters and flip-flop circuits 5003 are in a reset condition. If a conversion start signal is inputted into the strobe input terminal ST of a control circuit 5004, it will declare that answer it, and a control circuit 5004 makes logic 1 the output signal from the conversion terminate-signal terminal EOC, and is changing it.

[0219] A control circuit 5004 outputs the count load signal LD, makes an input digital signal load to the down counter 5001 synchronizing with the standup of Clock CK, and makes 0 load to the rise counter 5002. the down counter 5001 and the rise counter 5002 -- termination of the above-mentioned loading -- counting of a clock -- actuation is started.

[0220] A control circuit 5004 is late a term 1/2 round of a counter clock for the above-mentioned counter load signal LD, and outputs the set signal FR of a flip-flop circuit 5003 from it. a flip-flop circuit 5003 -- the borrow of the down counter 5001 --

since an output BO is logic 0, Input K is set to 0 1 and it changes Input J into a set condition synchronizing with the standup of a clock.

[0221] the down counter 5001 -- every arrival of a clock -- a down -- counting -- if it operates (-1) and enumerated data are set to 0 -- a borrow -- Signal BO is outputted. consequently, a borrow -- the input J of a flip-flop circuit 5003 changes to 0, and Input K changes with change in the logic 1 of Signal BO to 1. Consequently, a flip-flop circuit 5003 is reset synchronizing with the standup of a clock pulse.

[0222] in addition, the input digital signal Din -- decimal system -- the time of 0 -- the borrow of the down counter 5001 -- an output BO and the set signal FR of a control circuit 5004 will be outputted to the same timing. this example -- the borrow of the down counter 5001 -- in order to give priority to an output BO, AND circuit 5006 is formed, and the set signal FR of the flip-flop circuit 5003 from a control circuit 5004 is forbidden with this AND circuit 5006. Thus, when a digital signal Din is 0 in decimal system, a pulse is not outputted from a flip-flop circuit 5003. When a digital signal Din is one or more, the pulse which has the pulse width corresponding to each from the output Q of a flip-flop circuit 5003 is outputted. Thus, smoothness of the output signal by which Pulse Density Modulation was carried out is carried out with a low pass filter 5007, and analog signal Vout is formed.

[0223] the rise counter 5002 -- counting -- if actuation is continued and it becomes maximum, the carry signal CAR will be outputted. If the above-mentioned carry signal CAR is received, a control circuit 5004 will change the conversion terminate signal EOC to logic 0, and will end a series of conversion actuation. It waits for this conversion actuation termination, and the following digital signal is inputted. That is, when the above rise counters 5002 are formed, according to digital to analog actuation, by the conversion terminate signal EOC, an address signal is generated and the following input digital signal can be read.

[0224] As mentioned above, analog signal Vout corresponding to [when the input digital signal Din and the strobe were inputted / repeat the above actuation and] the input digital signal Din It forms. During the above-mentioned conversion actuation, a control circuit 5004 makes the conversion terminate signal EOC high-level, tells it outside, and it continues conversion actuation without answering for anything the strobe which disregarded this.

[0225] In addition, what is necessary is to form a repeat counter etc. and just to make it only the count of assignment repeat the above digital to analog actuation to a conversion start signal like one strobe, in mitigating the ripple component contained in the analogue conversion output Vout. What is necessary is to prepare a register in said this appearance and just to incorporate an input digital signal, when the input of a digital signal Din is not guaranteed during this repeat.

[0226] The example explained using drawing 47 - drawing 50 above can be widely used as a signal transformation circuit changed into a Pulse-Density-Modulation signal

from a digital signal besides a digital to analog circuit.

[0227] The fundamental block diagram of one example of the switch input circuit of a player 101 used for said digital signal delivery system is shown in drawing 51 .

[0228] As mentioned above, a player 101 is small and is made into a thin shape so that it may have IC memory card etc. and compatibility. So, it is made important to reduce the switches which direct a mode of operation. So, in this example, the signal 5103-1 - 51013-n which specify operating state 1 - operating state n are formed by the operating state control circuit 2 which receives ON / off signal of one key switch 5101. By doing in this way, mounting of an actuation switch is enabled at SU **-SU to which the above small and thin players 101 were restricted.

[0229] The block diagram for explaining one example of the concrete configuration of an operating state control circuit is shown in drawing 52 .

[0230] In this example, the ON time amount T of a switch 5101 is judged by the operating state control circuit 5102. The operating state control circuit 5102 will form the signal 5201-1 changed into Condition A, if a switch is only unconditionally made into an ON state to the ON time amount T of a switch 5101. If it decides on the ON time amount T of a switch 5101 beforehand and the operating state control circuit 5102 judges with it being smaller than fixed time amount M (M>T), it will form the signal 5201-2 changed into Condition B. And if it judges with the operating state control circuit 5102 being larger than fixed time amount M as which it decided on the ON time amount T of a switch 5101 beforehand (M<=T), the signal 5101-3 changed into Condition C will be formed. The following playback control action is realizable with the combination of the signal 5101-1 to 5101-3 which shows three above condition A-C.

[0231] The conceptual diagram for explaining the mode of operation is shown in drawing 53 .

[0232] A player 101 is made into a idle state 5302 just behind powering on. In this condition 5302, if a switch 5101 is made into an ON state, signal 5301a which shows the unconditional condition A to that ON time amount T is formed, and a player 101 will be in the playback condition 5303. In the state of [5303] this playback, it is made to change to the halt condition 5305, or returns to the idle state 5302 of a basis, or two kinds of choices are needed. Then, if a switch 5101 is again made into an ON state, signal 5301b which shows the above conditions A will be formed, it will go into the time amount judging 5304, and the judgment of time amount T then made into the ON state will be performed. If this judgment result is signal 5301c which shows Condition B, it changes a player 101 into the halt condition 5305. Or if the above-mentioned judgment result is signal 5301e which shows Condition C, a player 101 returns to the idle state 5302 of a basis. At the time of up Norikazu, since returning to the playback condition 5303 again in a idle state 5305 only has semantics, it is only made the ON state of a switch 5101, and returns to the playback condition 5303 by 5301d of signals

which show the above conditions A.

[0233] In directing two or more kinds of actuation with one switch, there is a fault to which the operating instructions become complicated. So, in this example, in order to make acquisition of those operating instructions easy, it displays whether it can be made to change with the inputs of Condition A – Condition C to what kind of condition by preparing light emitting diode etc. and a liquid crystal display component corresponding to the idle state 5302, the playback condition 5303, and the halt condition 5305 which were shown in drawing 51 , making the light switch on according to the present condition, and combining it and an arrow head as shown in this drawing. In order to attain low-power-ization, it is made just to make only fixed time amount which performs switch actuation perform, when a light emitting diode is used for this display action as an indicating equipment.

[0234] The block diagram of other one example explaining the concrete configuration of an operating state control circuit is shown in drawing 54 .

[0235] In this example, it replaces with the ON time amount T of the above switches 5101, and the count of ON of a switch 5101 is judged by the operating state control circuit 5102. The operating state control circuit 5102 forms the signal 5401-1 which carries out counting of the count of ON of a switch 5101, and is changed into Condition A if it is 1 time. The operating state control circuit 5102 forms the signal 5401-2 changed into Condition B, if the count of ON of a switch 5101 is 2 times. The following playback control action is realizable with the signal 5401-1 which shows such two conditions A and B, and the combination of 5401-2.

[0236] The conceptual diagram for explaining the mode of operation is shown in drawing 55 .

[0237] A player 101 is made into a idle state 5302 just behind powering on at said this appearance. In this condition 5302, if a switch 5101 is made only once into an ON state, signal 5501a which shows Condition A is formed, and a player 101 will be in the playback condition 5303. In the state of [5303] this playback, it is made to change to the halt condition 5305, or returns to the idle state 5302 of a basis, or two kinds of choices are needed. Then, if a switch 5101 is again made only once into an ON state, signal 5501b which shows the above conditions A will be formed, and it will change a player 101 into the halt condition 5305. Or if the above-mentioned switch 5101 is made twice into an ON state, signal 5501e which shows Condition B will be formed, and a player 101 will return to the idle state 5302 of a basis. It is made to make it change also to the idle state 5302 of a basis besides returning to the playback condition 5303 again from a idle state 5305 at the time of up Norikazu selectively in this example. For this reason, if a switch 5101 is made only once into an ON state in the halt condition 5305, signal 5501c which shows Condition A will be formed, and a player 101 will change to the playback condition 5303. If a switch 5101 is made into an ON state 2 times in a idle state 5305 at the time of up Norikazu, 5501d of signals

which show Condition B will be formed, and a player 101 will change to a idle state 5302. Also in this example, acquisition of actuation is made easy by [said] drawing a display device and an arrow head similarly corresponding to drawing 53 .

[0238] When reproducing, drawing 56 is the block diagram showing the concept of one example of enabling alternative playback and the so-called search by specifying a block reading with an actuation switch etc. beforehand, while dividing and (block division) recording a store circuit on the size of arbitration, when two or more contents which should be memorized exist. It adds to the data store circuit 5610 and the address counter 5611 for data. The storage address of the data store circuit 5610 To the address counter 5611 for data to decide, a block address The decoder circuit 5603 which decodes the content of the address counter 5602 for block addresses which specifies the address of the block-address store circuit 5601 for setting, and a block-address store circuit, and the address counter 5602 for block addresses, Furthermore, it consists of chatter killer circuits for removing the actuation switch 5607 for choosing the indicator 5604 and block which display this decoded content, and chatter etc. The RECSTOP signal (pulse of 100ns of width of face) which shows the PLAY signal (pulse of 100ns of width of face) which shows that storage/playback was started, and a storage halt is inputted into this circuit section.

[0239] Next, it is as follows when actuation of this circuit is explained. In order to make it intelligible here, the address counter 5602 for block addresses presupposes now that it was zero. In this condition, if it goes into a storage mode, data are memorized one by one from the 0th street of the store circuit 5610 for data. If a storage halt is now directed to the timing of arbitration, first, the increment of the address counter 5602 for block addresses will be carried out in the first transition of a RECSTOP signal (the content is set to 1), and the content of the address counter 5611 for data will be memorized by the 1st street of the block-address store circuit 5601 through a delay circuit 5608 for further 100ns (it becomes the start address of the 2nd data). Next, in order to memorize another data again, it goes into a storage mode, the 1st content of the block-address store circuit 5601 which remembered the point that a PLAY signal is outputted is loaded to the address counter 5611 for data as a start address as it is (set), and the sequential storage of the 2nd data is carried out. if a storage halt is directed hereafter -- ** -- it is alike and the content of the address counter 5611 for data is written in the block-address store circuit 5601 one by one. On the other hand, the procedure at the time of reproducing is as follows. Whenever it pushes the actuation switch 5607, the increment of the counter 5602 for block addresses is carried out and the content is displayed by the numerical indicator 5604 (a mere LED display is sufficient) through a decoder circuit 5603 to reproduce the block first made into the object, for example, the 2nd data. A depression will be stopped, if it continues pushing the actuation switch 5607 and the 1st street appears until the 1st street (the 2nd address is stored in the 1st street) made into the object

is displayed. Next, the start address as which a PLAY signal is outputted and the 1st content, i.e., the 2nd data, is remembered to be if playback is directed is loaded to the address counter 5611 for data (set), and read-out advances. In addition, when the above-mentioned indicator 5604 displays zero to reproduce the 1st data (the same is said of the storage), by stopping increment actuation of the address counter 5602 for block addresses, for a low-level and ****** reason, a PLAY signal passes through OR circuit 5606, and the all ZERO output of a decoder circuit 5603 clears the address counter for data. As a result, the data store circuit 5610 will perform playback (or storage) actuation from the 0th street, and the 1st data will be reproduced (or storage).

[0240] As mentioned above, according to this example, a block to read can be chosen as arbitration by easy actuation, and very user-friendly equipment can be offered. Moreover, another features of this example completely have the arbitrary block length, there is no futility and the data store circuit 5610 can be used efficient. This is what fully utilized the engine performance paying attention to the property of semiconductor memory, and is an example which shows the effectiveness of the equipment of this application. In addition, although the store circuit was divided into the data store circuit 5610 and the block-address store circuit 5601 and was explained here, you may arrange on the same memory.

[0241] The conceptual diagram of one example of the storage region management method of the store circuit 701 of a player 101 is shown in drawing 57 .

[0242] In order to use efficiently the storage capacity of the store circuit 701 carried in the player 101 to two or more kinds of information, a store circuit 701 is divided into a table-of-contents field and a data area. Although especially a table-of-contents field is not restricted, it has four tables of contents 5701a-5704a, and storing of block addresses BA0-BA3 is enabled at each. The above-mentioned tables of contents 5701a-5704a are chosen by program select signal PSL1 and PSL2 grade, and writing and read-out of the block address BA 0 and BA1 grade are made possible.

[0243] For example, in the above digital signal delivery systems, if a player 101 is connected to a terminal unit 100, a terminal unit 100 will read the block address which accesses a table-of-contents field and is confirmed. Thereby, a terminal unit 100 can know the free area of the store circuit 701 in a player 101. And while making an empty table of contents memorize a block address, a free area is made to memorize a digital signal, if the digital signal which newly wins popularity and is passed is specified. If tables of contents run short or empty memory capacity runs short to the digital signal received and passed, the digital signal [finishing / storing] which may display and eliminate that will be made to choose, it will be eliminated, and a new digital signal will be inputted. at this time, reading appearance also of the digital signal [finishing / storing] memorized by the player 101 is carried out, and address assignment is anew performed so that there may be no opening in storage capacity according to the

storage capacity of a new digital signal.

[0244] Table-of-contents 5701a is accessed by program select signal PSL1, the block address BA 0 stored there is read, and it is made to set to an address counter 703 in this drawing. For example, read-out is started sequentially from the address with which ID code 5701i of the head of the block was stored as the block address BA 0 set to the address counter 703 like the continuous line of this drawing is data block 5701d of the start address of a data area. And although not restricted especially, end mark 5701e is stored in the last address of data, and read-out is terminated by detection of this end mark 5701e. With this configuration, since what is necessary is just to make a table of contents memorize only a start address, address information can be reduced.

[0245] Moreover, a table of contents 5702 is accessed by program select signal PSL2, the block address BA 2 stored there is read, and it is made to set to an address counter 703. For example, if the block address set to the address counter 703 like the dotted line of this drawing is an intermediate block, read-out is started sequentially from the address with which ID code 5702i of the head of the block was stored. And end mark 5702e is stored in the data 5702d last address like the above, and read-out is terminated by detection of this end mark 5702e.

[0246] For example, if an opening is made between the data blocks in which two kinds of programs were stored as mentioned above by elimination of the digital signal corresponding to table-of-contents 5701a etc., a terminal unit 100 will write in the digital signal corresponding to it while changing a block address BA 2 into the address of end mark 5701e of the data area corresponding to table-of-contents 5701a for the block address BA 2 of table-of-contents 5702a. By doing in this way, the empty remaining area can be continuously used for the digital signal corresponding to the program which newly wins popularity and is passed.

[0247] In addition, when a player 101 is connected to a terminal unit 100, a table-of-contents field and a data area are cleared in principle, and a new digital signal may be made to be stored. In this case, a program to leave may specify the prohibition on elimination as a player 101 side, or may specify an elimination prohibition program in delivery actuation of the digital signal by the side of a terminal unit 100.

[0248] The conceptual diagram of other one example of the storage region management method of the store circuit 701 of a player 101 is shown in drawing 58 .

[0249] In this example, the table-of-contents store circuit 5801 and the data store circuit 5802 are made to perform the storage management of a digital signal. The table-of-contents store circuit 5801 enables storing to a maximum of four kinds of digital signals (program) like a table of contents 1 thru/or a table of contents 4. The table-of-contents store circuit 5801 is made to also memorize the table-of-contents information that a start address is made to only memorize like said example, besides an ending address besides a thing, or an ID code. Although especially this

table-of-contents information is not restricted, it consists of text, forms a liquid crystal display in a player 101, and enables the display of the content of the program in an alphabetic character.

[0250] Each table of contents of the table-of-contents store circuit 5801 and the data area of the data store circuit 5802 are performed to arbitration by storage sequence etc. like data 2, data 1, data 4, and data 3 from the start-address side of the data store circuit 5802. That is, a digital signal is memorized [as opposed to / the order specified previously / data store circuit 5802].

[0251] The important section block diagram of one example of the player 101 at the time of adding the above-mentioned table-of-contents function is shown in drawing 59 .

[0252] The switch 5907 for table-of-contents assignment (program assignment) other than the above switches 5908 for motion control is formed in a control circuit 5906. Although not restricted especially, if this switch 5907 is made into an ON state, the pulse of +1 will be supplied to the table-of-contents address counter 5901, and access of the table-of-contents store circuit 5801 will be performed. The table-of-contents information by which reading appearance was carried out from the table-of-contents store circuit 5801 is stored in the table-of-contents register 5909, and character representation, such as a title, is performed by the liquid crystal display 5910.

[0253] The start address by which reading appearance was carried out from the table-of-contents store circuit 5801 is set to the address counter 5902 of the data store circuit 5802, and an ending address and an ID code are loaded to registers 5903 and 5904, respectively. An ID code is told to a control circuit 5906, it is decoded, and automatic setting, such as said sampling frequency, a data length, a stereo / monophonic playback, is performed.

[0254] The address signal outputted by the above-mentioned address counter 5902 is supplied also to the comparator 5905 besides being used for access of the data store circuit 5802. The last address loaded to the above-mentioned register 5903 is told to the input of another side of this comparator 5905. Since a comparator 5905 detects this and inputs a terminate signal into a control circuit 5906 after read-out of the digital signal (data) corresponding to the table of contents by which assignment was carried out [above-mentioned] is completed by this, read-out actuation of a series of digital signals will be completed.

[0255] In the above table-of-contents function, since a binary address counter can use as it is if it is made the Nth power individual of 2, although the number of tables of contents is arbitrary besides 4, selection becomes easy. Moreover, when the table-of-contents store circuit 5801 is formed independently [the data store circuit 5802], since each can be accessed in parallel independently, control of an address counter becomes easy. In addition, it cannot be overemphasized that the

above-mentioned table-of-contents store circuit 5801 may be what is constituted like the example of above-mentioned drawing 57 using the fixed storage region of the data store circuit 5802.

[0256] Drawing 60 shows one example of the player 101 by this invention like above-mentioned drawing 7 . This example shows IC-izing or hybrid-IC-ized 1 chip integrated circuit 6001 for the multiplexer 702 except the part 701 of an alternate long and short dash line within the limit, i.e., the store circuit of a player 101, an address counter 703, a control circuit 704, the parallel/serial-conversion circuit 705, the low pass filter 706, the digital to analog circuit 707, and the amplifying circuit 708. This 1 chip integrated circuit is equipped with the signal and the terminal which realizes data transfer of the above-mentioned digital signal delivery system, the signal and the terminal which controls the above-mentioned store circuit, the signal and the terminal which outputs an analog sound signal, the signal and the terminal which supports actuation to 1 chip integrated circuit, the signal and the terminal in which the condition of 1 chip integrated circuit is shown, and the signal and the terminal which supply power to a 1 chip integrated circuit. Moreover, the configuration of 1 chip integrated circuit does not need to include all the functions shown above, and is not limited especially.

[0257] According to this example, it is miniaturized, so that all the circuits of a body that contain a cell in the part of the lug of the headphone with a micro book which the operator etc. uses can be mounted, and it is power consumption at the standby time, and about 20mW is surveyed at the time of about 50 microwatts and playback, it is small and extremely little equipment of power consumption can be realized. Even if this uses the carbon button form lithium cell of small capacity (180mAh) for a power source and it leaves the data beyond continuation 30 hour memorized [which memorized and playback-operated] as it is, it has suggested that it is possible to make it reproduce 450 days after. Moreover, by the technical progress of a cell, these values have room to be improved substantially, and rear-spring-supporter record can be held or they can realize playback actuation or the small and lightweight equipment of hundreds of hours or more in several.

[0258] In addition, when a control circuit is dedicated to 1 chip integrated circuit, there is a problem to which the storage capacity of the store circuit which it remains as it is and can be controlled will be restricted. In order to solve this problem, as shown in drawing 61 , the storage capacity of a store circuit is extensible by preparing the signal for an escape, and the terminal in the control signal and terminal of a store circuit as an option. For example, as shown in drawing 60 , when the address which the address counter 703 stored in 1 chip integrated circuit generates is 23 bits (data are made into 8 bits), the memory capacity of a store circuit becomes a maximum of 8,388,608 bytes. What is necessary is to establish the address escape circuit which consists of extended multiplexers 6102 which carry out the same actuation as the

extended address counter 6101 which is interlocked with the internal address counter 703 and operates, and the internal multiplexer 702 in the exterior of 1 chip integrated circuit, as shown in drawing 61 , and just to extend the address given to a store circuit to 24 bits to double storage capacity 16,777,216.

[0259] The block diagram of the self-test circuit for distinguishing automatically the defective bit of the store circuit in a player 101 in drawing 62 , and skipping a defective bit to it is shown.

[0260] In the player shown in drawing 7 , the self-test circuit is added to the store circuit 701 on the outskirts. the data inputted into a store circuit 701, and two kinds of data patterns for a store circuit test -- it consists of the buffer circuit 6204 for connecting to a store circuit the output of the ternary counter 6201 for giving a selection signal to the multiplexer 6202 and this multiplexer 6202 which choose "AA" and "55", and the above-mentioned multiplexer 6202, a delay circuit 6206, an address counter 703, a comparator 6203, first in first out memory 6207, etc. this -- a circuit -- the section -- I/O -- a signal -- a terminal unit -- 100 -- from -- input data -- a store circuit -- from -- output data -- moreover -- a control circuit -- from -- a store circuit -- writing -- a strobe signal -- (-- WE --) -- storage -- /-- playback -- inside -- being shown -- RUN -- a signal (RUN) -- and -- two -- a kind -- a store circuit -- a test pattern -- data -- " -- AA -- " -- " -- 55 -- " -- inputting -- having . In addition, skip address output and playback clocked into are the signals for skipping and reading the defect part (defective address) of a store circuit at the time of playback actuation. It writes in, immediately after stored data changes, and a strobe signal (WE) inputs with the pulse width for 100ns (repeat frequency is 8kHz), makes the ternary counter 6201 a cleared condition through OR circuit 6213, passes through OR circuit 6214 and also negative OR circuit 6205, and is connected to the control terminal of a buffer circuit 6204, and WE (write enable) of a store circuit. A buffer circuit is a hi-z state, when this control terminal of 6204 is high-level. It is the component which is begun when this control terminal is set to a low level and by which an input is reflected in an output terminal. The data terminal (DIO) of one store circuit If WE terminal is high-level, the content of the appointed address will be outputted, if WE terminal is set to a low level, the above-mentioned DIO terminal will change to the condition in which a data input is possible, and it will be written in the address specified by the data input of this DIO terminal. Therefore, if the data of the input side of a buffer circuit 6204 and an output side immediately after the above-mentioned WE pulse signal returns high-level (accuracy after 50ns progress of the access time of a store circuit) are in agreement and the above-mentioned data comrade is not [it means that data were normally written in the store circuit and] in agreement, it is shown that data were not normally written in the above-mentioned store circuit. Forming a comparator 6203, in order to perform such a judgment, Y output of this comparator 6203 is made into the logical organization of an inequality output which

becomes high-level when the content of A input terminal and the B input terminal is not in agreement, and it considers Y output of this comparator as one input of AND circuit 6210. Here, the output of above-mentioned NOR circuit 6205 is further inputted also into the pulse delay circuit 6206 with a logical-NOT function, becomes WE' pulse which was able to be sent for about 200ns by this delay circuit 6206, and turns into another input of AND circuit 6210. If the above-mentioned inequality output is a low level at this time, namely, when data are normally written in a store circuit 701, nothing will be outputted to the output of above-mentioned AND circuit 6210. The above-mentioned ternary counter 6201 is reset at the time of the input of WE pulse (priority is given to clear actuation although the pulse is simultaneously inputted also into clocked into CP), and the QA output QB output of this ternary counter 6201 has a low level here. Since the multiplexer 6202 has chosen pattern"AA" (set to 10101010 from the 7th power bit side of 2 in a hexadecimal notation and a binary system at order), it will call the data normally written in the above-mentioned store circuit 701 the 1st test pattern. Then, since QB output (2 1st power bits) of the ternary counter 6201 is a low level, this output becomes high-level in the logic indeterminate circuit 6216. AND circuit 6211 passing above-mentioned WE', and counting up the ternary counter 6201 via OR circuit 6214 -- a multiplexer 6202 -- test pattern "55" (a hexadecimal notation --) a binary system -- the 7th power bit side of 2 -- order -- 01010101 -- becoming -- it chooses, the output of above-mentioned OR circuit 6214 turns into an input of negative OR circuit 6205 simultaneously, and it acts as a write pulse to a store circuit. henceforth, test pattern "55" -- when it is further written in normally also in any of stored data (store circuit input data), above-mentioned AND circuit 6211 is forbidden, a round loop formation which was described above (since QB output of the ternary counter 6201 becomes high-level) will be opened, WE' pulse will pass AND circuit 6212 instead, and will count up an address counter 703, and will wait for the next write-pulse (WE) input from a control circuit. Moreover, in the case where data were not written in normally [Y output (inequality output) of the above-mentioned comparator 6203] to high level 701, i.e., a store circuit, the above-mentioned WE' pulse will pass AND circuit 6210, and will repeat writing and the thing same since it has inputted into negative OR circuit 6205 and OR circuit 6213 simultaneously as actuation when the above-mentioned WE pulse is inputted for the content of the address counter 703 at that time once again to the first in first out memory 6207. In addition, this repetition actuation is continued until data are normally written in a store circuit 701 (the time amount which this repetition actuation takes is about 300ns). Moreover, the number of cycles actually permitted since WE input period is about 125 microseconds In the case repeated with the 1st pattern check, i.e., error generating at the time of "AA" pattern writing, it is about 400 times, and becomes about 200 times in the case repeated at the 2nd pattern check, i.e., error generating at the time of "55" pattern writing.

[0261] Since according to this example the semi-conductor memory chip thrown away by inspection can be used although the several [only] bits memory cell of the mass memory cells of megabit classes, such as 4 megabits or 16 etc. megabits, is poor therefore, equipment very cheap as a result can be offered. It is fundamental thought for the thought described here to inspect, before writing in, and to utilize a defect bit using that result, and it cannot be overemphasized that various deformation and application are possible using this concept. For example, when the defect bit by which the inspection result was fixed to "1" when writing in "1" is detected, there is also a method of using it as "1" as it is.

[0262] In addition, the simple self-test circuit by the method checked while writing in a store circuit only using write-in data can be constituted by fixing actuation of the multiplexer 6202 in drawing 62 (the ternary counter 6201 carrying out and a low level and QB output being fixed for GA output high-level).

[0263] Moreover, especially this example becomes effective especially, when a sound recording function (there are a case of voice, other images, medical information, etc.) is added to the above-mentioned player.

[0264] It is based on this invention, digital signal delivery is carried out, and the appearance of one concrete example of a system is shown in drawing 67 . drawing -- setting -- the same part as drawing 1 , drawing 3 , drawing 7 , drawing 10 , or drawing 59 -- the same number -- **** -- detailed explanation is omitted by things.

[0265] 1001 shows the small store circuit section which consists of a memory card or an IC card etc. which mainly consists of semiconductor memory. The parents for memory duplication, a child, and a grandchild type carry out digital signal delivery, and this example shows a system in order to add a function to a player 101 further. It has the 2nd clock of the high speed which has the 1st clock which is the sampling frequency of the analog-to-digital-conversion circuit at the time of external input signal sound recording in the terminal unit 100 of this drawing, and transmits an audio digital signal to a player 101 from a terminal unit 100. Furthermore, a player 101 has the 3rd clock which is the sampling frequency of the digital to analog circuit at the time of playback.

[0266] Moreover, a player 101 has the 4th high-speed clock for transmitting a digital signal to the store circuit section from this player. In addition, when a terminal unit 100 and a player 101 are used in the state of connection, this 4th clock may use the 2nd clock. The 4th clock can be excluded at least in that case. The 1st and the 3rd clock for sound recording or playback can each carry out adjustable in these clocks. music -- an audio sampling frequency -- a high speed -- it can do -- more -- high -- a tone quality playback sound is expectable. Moreover, in conversation, a sampling frequency is made into a low speed and a memory activity can be saved.

[0267] For example, transfer record is carried out with the 4th high-speed clock, and-izing of the recorded content can be carried out [****] to the small memory

card or small IC card which chooses the voice file of arbitration from the terminal unit 100 which is parents with the utilization gestalt of this drawing, carries out high-speed writing with the 2nd clock which transmits information to the player 101 of the magnitude of electronic notebook extent which is a child, and becomes a grandchild in the store circuit section further with other players 101 or an electronic notebook.

[0268] Moreover, it is also considered that a manufacture and software-development manufacturer side offers speech information, a processing program, etc. in the form of a memory card or an IC card. Furthermore, an option function, such as text-izing a sound signal, is added to a player 101, and it becomes possible to memorize a text to store circuit circles etc. In addition, a grandchild's card is not limited to the card which used semiconductor memory, and the media activity of various micro light, a magnetic disk, etc. is also considered in the future.

[0269] In addition, the player of this example is not limited to this, although the store circuit section shown in drawing 10 is the thing of an attachment-and-detachment type. In transmitting information to a player 101 from a terminal unit 100, the player in the condition of having equipped with the store circuit section is mounted in the player insertion opening 6701 of a terminal unit 100, and it transmits the selected information at high speed to a player. At this time, information which should be transmitted out of the information accumulated in the storage section 303 by actuation of the actuation switch group 6702 of a terminal unit 100 is chosen. At the time of playback, a player is reproduced by the cash drawer and independent from a terminal unit 100. Moreover, this example shows the comparatively large-scale example aiming at deferring to the firm of a town, the canteen of a station, etc.

[0270] It is based on this invention, digital signal delivery is carried out, and the appearance of other one concrete example of a system is shown in drawing 68 . drawing -- setting -- the same part as drawing 1 , drawing 3 , drawing 4 , drawing 7 , drawing 10 , drawing 59 , or drawing 67 -- the same number -- **** -- detailed explanation is omitted by things.

[0271] The control unit to which 406 performs a loudspeaker and 6702 performs record playback is shown, and the equipment with which terminal unit 100 the very thing also has a sound recording regenerative function is shown. For example, a terminal unit 100 is a multifunctional form voice recorded message sender for telephone which has functions, such as radios, such as FM, AM, and TV, an optical disk, a magnetic disk, a digital audio tape, and timer reservation sound recording, at least, and can carry out the acceleration escape of the multimedia-izing further by this invention's carrying out digital signal delivery, and adding a system.

[0272] It cannot be overemphasized that the configuration of the above-mentioned terminal unit 100 can deform also in deferment or a carriable form according to an environment. Moreover, this invention can carry out digital signal delivery, a system can be introduced into a telephone etc., and a lot of information can also come to

hand by the housesitting sound recording function.

[0273] In addition, this example shows the comparatively small example for home use.

[0274] It is based on this invention, digital signal delivery is carried out, and the appearance of the most characteristic concrete example of a system is shown in drawing 69 . drawing -- setting -- the same part as drawing 1 , drawing 3 , drawing 4 , drawing 7 , or drawing 10 -- the same number -- **** -- detailed explanation is omitted by things. This example has the following descriptions in order to realize that it can be operated easily [whom]. Although not illustrated especially in this example, if a touch panel is adopted as a liquid crystal display 303 and the function of operating instruction and an actuation switch is expressed on this screen, the actuation switch is lost as much as possible by hierarchization of an actuation screen etc. (only in case of the below-mentioned check switch). Thereby, the user-friendliness to a user is improved substantially. Furthermore, mechanical processing which prevents reverse insertion to player insertion of a terminal unit 100 is performed. Moreover, in order to prevent the false drop of a user's information, the check switch 6901 is formed. Information is transmitted to a player 101 in an instant by pushing and going down the check switch 6901 by the above-mentioned audition function, after checking the selected information. Moreover, the result and player insertion acknowledgement message to which the terminal unit 100 other than a normal operation screen checked the condition of the cell 710 in a player 101 are also displayed on a display panel 303.

[0275] Furthermore, a terminal unit 100 and a player 101 are connected by the connector according to JEIDA specification or JEIDA specification.

[0276] the switch whose player 101 of this example turns on / turns off a power source, and the above -- one pushbutton switch which directs a late mind / switch which already hears it and specifies the mode, the switch which specifies loudness rating mode, and playback / halt / halt actuation is formed.

[0277] moreover -- although the monochrome display of an alphabetic character and the graphic screen was carried out to the liquid crystal display 303 of the terminal unit 100 of this example, even if this invention moreover carries out color display of a static image or the dynamic image, without being influenced by this It is satisfactory in any way. The operation effectiveness acquired from the above example is as follows. Namely, (1) In delivery of a digital signal, direct continuation of the player as a terminal unit is carried out to a digital signal supply source corresponding to one to one, and while making a reception store circuit memorize the specified digital signal as it is, the digital signal made to memorize by the player independent is reproduced. With this configuration, the effectiveness that a player can remain as it is and can demonstrate worth of the digital signal delivered in the digital signal since it is reproduced by reception and independent is acquired.

[0278] (2) The effectiveness that the digital signal which wins popularity as goods etc. and is passed by the above (1) can perform the processing, manufacture, and

construction of a sale system easily is acquired.

[0279] (3) Since it is that in which a player has the function in which accepted the value as goods etc. in the very thing, and only reproducing it was only simplified in the digital signal received and passed by the above (1), and the configuration of a player is easy and actuation is also easy, the effectiveness that it can treat to anyone is acquired.

[0280] (4) delivering the digital signal which formed the terminal unit which carries out the reception storage of the digital signal through a communication line or a suitable storage if needed from the supply origin of a digital signal, was connected with the player through the connector and specified as this -- the sale system of the digital signal as goods etc. -- a high speed -- and the effectiveness that it can carry out rationally is acquired.

[0281] (5) The effectiveness that delivery of an efficient digital signal is realizable is acquired by making the buffer memory constituted by the semiconductor memory in which rapid access is possible memorize the digital signal updated with a digital signal or the passage of time with many amounts of delivery, using the magnetic disk memory equipment which has comparatively big memory capacity as a terminal unit as a backup memory.

[0282] (6) The effectiveness that the simplification of a player and a deployment of a store circuit are attained is acquired by performing management of the storage area of the store circuit in a player besides delivering and receiving a digital signal with the supply origin which gave microcomputer ability and minded management and the communication line of the above-mentioned magnetic disk memory or buffer memory as a terminal unit.

[0283] (7) as a terminal unit -- a part of digital signal -- the effectiveness that the selection mistake of the target digital signal is prevented, or selection of the target digital signal can be made easy is acquired by adding the function in which a monitor is possible for a part only within fixed time amount.

[0284] (8) The effectiveness that it can be simplified like storage and playback of the function in a player is acquired by limiting to speech information by making the digital signal delivered into a digital sound signal.

[0285] (9) While delivering the various digital signals corresponding to an information program by adding an ID code to the digital signal delivered, and carrying out automatic assignment of the playback conditions in a player, the effectiveness that the user-friendliness can be improved is acquired.

[0286] (10) By making the card-like store circuit section removable from a player body, various kinds RAM, EEPROM, or ROM can be used as a store circuit, and the effectiveness that diversification of a function is attained is acquired.

[0287] (11) The external configuration and connector of a player have an existing memory card and compatibility, and the effectiveness that an internal store circuit

can be made usable at an existing memory card and an existing EQC is acquired.

[0288] (12) The effectiveness that multi-functionalization of a player and amplification of an application can be aimed at is acquired by the above (10) and (11).

[0289] (13) By adding a security function to the input and/or output actuation of a store circuit at a player according to the coincidence detecting signal of a password or a password, since easy KOPIYA, tapping, etc. can be prevented, the effectiveness that commodity value of the digital signal received and passed can be made high is acquired.

[0290] (14) By making removable storage of the shape of a card thin as a part of store circuit section of a player, since the escape of storage capacity and playback of the program constituted by various kinds ROM are also attained if needed, the effectiveness that various functions are realizable is acquired.

[0291] (15) The effectiveness that security is made by the easy configuration is acquired from taking the configuration which is made to reverse at least 1-bit digital signal of the data input of the store circuit of a digital signal and/or data output, or the address input section, or is replaced with other bits as the above-mentioned security method.

[0292] (16) The effectiveness of the ability to make the digital signal as two or more kinds of information storing in a store circuit efficiently is acquired by preparing the storage region or table-of-contents store circuit which memorizes the table-of-contents information which includes the storing address corresponding to two or more digital signals in a player, and the data area or data store circuit accessed by the above-mentioned storing address.

[0293] (17) From it being made to specify the mode of operation which consist the motion control of the above-mentioned player of a class with the ON time amount of one key switch, or the combination of the count of ON, the effectiveness that small [of a player] and thin shape-ization are realizable is acquired.

[0294] (18) The effectiveness that the jarring quantizing noise of a silent period is removable is acquired by detecting the silent period of the digitized sound signal and transposing compulsorily the digital signal inputted into a digital to analog circuit to the signal corresponding to 0 alternating current level in the silent period.

[0295] (19) The effectiveness that an exact silent period is detectable according to the content of the program of a digital signal is acquired by forming based on the output signal of the comparator of the couple which performs the size comparison with the digital signal corresponding to the level of the positive/negative amphipathy whose adjustment of detection of a silent period was enabled consider that is silent respectively, and the digital signal reproduced.

[0296] (20) The effectiveness that maintenance ********** becomes possible about the quality of loud sound is acquired by detecting the silent period of the digitized sound signal and carrying out amplification extension of the meantime.

[0297] (21) The effectiveness that the easy configuration which ** substantially renewal actuation of the address of the store circuit where the digital signal was stored compared with normal operation and to say can realize ******, with the quality of loud sound maintained is acquired.

[0298] (22) The effectiveness that ****** becomes possible is acquired by detecting the silent period of the digitized sound signal and shortening the meantime, maintaining the quality of loud sound.

[0299] (23) The effectiveness that the easy configuration of making quick renewal actuation of the address of the store circuit where the digital signal was stored compared with normal operation can realize ******, with the quality of loud sound maintained is acquired.

[0300] (24) While a data compression becomes possible by transposing the silent period of a digital signal to silent code information and a silent hour entry, the effectiveness that ****** or ****** can be performed is acquired by expanding the above-mentioned hour entry, lengthening silent time amount, reproducing, or disregarding it and reproducing by the addition of an easy circuit besides making the silent time amount corresponding to the hour entry.

[0301] (25) By combining at least two continuous digital signals corresponding to almost forward maximum and almost negative maximum as a silent code, the effectiveness that discernment from a digital sound signal and a silent code can be performed easily is acquired.

[0302] (26) The effectiveness that the dead time which playback with ****** mode takes can be abolished is acquired by setting up the maximum silent time amount and preparing the function restricted so that the silent period expanded with ****** actuation may not exceed the above-mentioned maximum silent time amount.

[0303] (27) It asks for difference with the data inputted as the sampling data in front of one, in being larger than the maximum of the sign into which difference is compressed, it outputs maximum, and output the data which were made to output a subtraction result and were compressed when small, and perform a data compression. By this method, the effectiveness that on comparatively quiet data and easy configurations [distribution / the amplitude or / frequency / time amount], such as subtraction and addition, can perform a data compression with high fidelity is acquired like an acoustic signal.

[0304] (28) The effectiveness that a data compression and an expanding circuit can be realized by easy circuits, such as a subtractor, an adder, a register, and a comparator, and can also stop the power consumption small by the above (27) is acquired.

[0305] (29) By using the above data-conversion methods and circuits, the effectiveness that small lightweight-ization of the player which reproduces the acoustic signal memorized in the store circuit is realizable is acquired.

[0306] (30) counting corresponding to [make a store circuit memorize a digital input signal, receive a conventional-time pulse, and] the maximum of a digital input signal -- the effectiveness that the analog signal of the quality of loud sound can be acquired is acquired by making multiple times repeat the actuation which carries out the comparator comparison of the digital signal by which storage was carried out [above-mentioned] with the output of the counter circuit which operates, and forms a Pulse-Density-Modulation signal with a repeat counter.

[0307] (31) The digital signal supplied by the fixed period corresponding to the maximum of a digital signal is inputted into a down counter, and the effectiveness that the Pulse-Density-Modulation signal corresponding to the above-mentioned digital signal can be acquired by the easy circuit of making a conventional-time pulse form is acquired.

[0308] (32) counting corresponding to [in response to the above-mentioned conventional-time pulse] a digital input signal for the fixed period corresponding to the maximum of the above-mentioned digital signal -- the effectiveness of the ability to make the digital signal corresponding to address translation actuation inputting with an easy configuration is acquired by forming by the rise counter circuit which operates.

[0309] (33) By forming the digital to analog circuit except a store circuit, a low pass filter, an amplifying circuit, a control circuit, etc. into 1 chip integrated circuit among the functions which constitute the above-mentioned memory card with a playback device, it is very small and extremely small ** of power consumption can be offered. Moreover, it can mass-produce now easily and cost is also lowered.

(34) In the above-mentioned memory card with a regenerative function, by preparing the function which carries out the self-test of the store circuit, and skips a defective bit, the defect memory chip conventionally thrown away by inspection can be used, and very cheap equipment can be offered.

[0310] (35) By fitting the above-mentioned player to JEIDA specification, compatibility with the existing memory card is securable.

[0311] Although invention made from this invention person above was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which the invention in this application is not limited to said example, and does not deviate from the summary. For example, in a digital signal delivery system, it may be provided by onerous to the specific person who directs a player as one of the services, such as a securities firm besides what sells a digital signal as one goods, and a financial insurance company, etc. Or the whole digital signal may be used for delivery of periodical or information required for arbitration by package deal. Moreover, as long as transfer with a sound signal is possible for a digital signal like data required for linguistic study or the memorization for [various] taking an examination, it may be anything.

[0312] Furthermore, it replaces with the conventional newspaper, a weekly magazine,

etc. using a type by the above digital signal delivery systems, and using a digital sound signal, in various information and amusement, it is timely and offer, then a thing [a thing] said and which build very efficient near future-media are also possible.

[0313] It is good for a player also as a configuration which prepares KONETAKU which can connect the ROM card or RAM card for an escape. In this case, in order to prevent the thickness of the player itself becoming thick, as for the above-mentioned ROM card or a RAM card, it is desirable to consist of thin plastic cards with which the memory chip was built in. A ROM card will become convenient for a music program, linguistic study, etc. The above-mentioned RAM card serves as a means effective in the escape of store circuit capacity. For example, when receiving the long music program of performance time amount etc., the above-mentioned RAM card becomes effective.

[0314] The configuration of the terminal unit used for a digital signal delivery system and a player, a function, etc. can take various operation gestalten. A unnecessary flash memory (EEPROM), various kinds ROM, etc. are further sufficient as a cell because of storage maintenance, and the store circuits built in a player may be what uses the static mold RAM besides said false static mold RAM, the thing constituted from a dynamic mold RAM and an automatic refresh circuit, and a thing using rewritable small thin optical disk memory.

[0315] The text, the image information or the sound signal, the alphabetic character, or image information other than the above sound signals may combine a digital signal. Thus, a display is needed in order to reproduce text and speech information. What is necessary is just to use the liquid crystal display in which the formation of small lightweight is possible with a thin shape especially as a display, although not restricted.

[0316]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly. That is, in delivery of a digital signal, direct continuation of the player as a terminal unit is carried out to a digital signal supply source, and while making a reception store circuit memorize the specified digital signal, the digital signal made to memorize by the player independent is reproduced. in this system, since it reproduces by reception and independent while the player has been the gestalt of a digital signal, it comes out as it is and worth of the digital signal received and passed is demonstrated -- things can be carried out. And since the configuration of a player is easy and actuation is also easy, it can be treated to anyone, while it can perform the processing, manufacture, and construction of a sale system easily with the gestalt of a digital signal, since delivery is good. moreover -- while maintaining the quality of loud sound by detecting the silent period of the digitized sound signal and making it ****** by making the silent period expand -- ****** playback -- it is already heard and playback can be realized. The amplitude and frequency distribution can realize a data compression with high fidelity,

and expanding processing by easy circuits, such as a subtractor, an adder, a register, and a comparator, in comparatively quiet data with time amount like an acoustic signal. And by carrying out the multiple-times loop of the signal of the pulse width corresponding to a digital input signal in 1 time of a signal transformation period, and being made to perform it, since the ripple when carrying out smoothness can be decreased substantially, the analog signal of high quality can be acquired. Moreover, since it is very small, extremely little equipment of power consumption is realized and mass production becomes easy by forming a player into 1 chip integrated circuit, cost is also lowered, a defect memory chip becomes usable by the self-checking function, and very cheap equipment can be offered.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the important section block diagram showing one example of the digital signal delivery system concerning this invention.

[Drawing 2] It is the block diagram of the input section of the terminal unit of drawing 1.

[Drawing 3] It is the block diagram of the storage section of the terminal unit of drawing 1.

[Drawing 4] It is the block diagram of the output section of the terminal unit of drawing 1.

[Drawing 5] It is the important section block diagram of the data input section of a player.

[Drawing 6] It is the important section block diagram of the data output section of the terminal unit of drawing 1.

[Drawing 7] It is the block diagram showing one example of the player used for the digital signal delivery system concerning this invention.

[Drawing 8] It is the top view showing one example of the mounting substrate which constitutes the above-mentioned player.

[Drawing 9] It is the side elevation showing one example of the mounting substrate in the condition of being governed by the case.

[Drawing 10] It is the top view showing other one example of a player.

[Drawing 11] It is the block diagram showing the player body of drawing 10, and one example of the store circuit section.

[Drawing 12] It is the block diagram showing one example of the current supply method of a player.

[Drawing 13] It is the block diagram which one example of the digital signal transmitted

to a player from a terminal unit shows.

[Drawing 14] It is the block diagram showing one example of the player corresponding to the digital signal with which the ID code of drawing 13 is inserted.

[Drawing 15] It is the circuit diagram showing one example of the quantizing-noise clearance circuit concerning this invention.

[Drawing 16] It is a wave form chart for explaining an example of actuation of the quantizing-noise clearance circuit of drawing 15 .

[Drawing 17] It is the circuit diagram showing one example of the security circuit used for the digital signal sale system concerning this invention.

[Drawing 18] It is the circuit diagram showing other one example of the security circuit used for the digital signal sale system concerning this invention.

[Drawing 19] It is the circuit diagram showing other one example of the security circuit used for the digital signal sale system concerning this invention.

[Drawing 20] It is the circuit diagram showing other one example of the security circuit used for the digital signal sale system concerning this invention.

[Drawing 21] It is the circuit diagram showing one example of further others of the security circuit used for the digital signal sale system concerning this invention.

[Drawing 22] It is the concrete circuit diagram showing one example of the rearrangement circuit used for the security circuit of drawing 21 .

[Drawing 23] It is the circuit diagram showing one example of the security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention.

[Drawing 24] It is the circuit diagram showing other one example of the security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention.

[Drawing 25] It is the circuit diagram showing one example of further others of the security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention.

[Drawing 26] It is the circuit diagram showing one example of further others of the security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention.

[Drawing 27] It is the concrete circuit diagram showing one example of the rearrangement circuit used for the security circuit of drawing 26 .

[Drawing 28] It is the circuit diagram showing one example of further others of the security circuit suitable for the anti-copying used for the digital signal sale system concerning this invention.

[Drawing 29] It is the concrete circuit diagram showing one example of the rearrangement circuit used for the security circuit of drawing 28 .

[Drawing 30] It is the block diagram showing ****** concerning this invention, and one example of the digital sound signal processing circuit which realized ******

playback.

[Drawing 31] It is the block diagram concerning this invention in which already hearing it and showing concrete 1 example of a circuit.

[Drawing 32] It is the block diagram showing concrete 1 example of the ****** circuit concerning this invention.

[Drawing 33] Drawing 31 already hears it and it is a wave form chart of operation corresponding to a circuit.

[Drawing 34] It is a wave form chart of operation corresponding to the ****** circuit of drawing 32 .

[Drawing 35] It is the block diagram concerning this invention in which already hearing it and showing other one example of a circuit.

[Drawing 36] It is the block diagram showing other one example of the ****** circuit concerning this invention.

[Drawing 37] It is the block diagram showing other one concrete example of the ****** circuit concerning this invention.

[Drawing 38] It is a conceptual diagram of operation for explaining an example of actuation of the ****** circuit shown in drawing 37 .

[Drawing 39] It is a conceptual diagram of operation for explaining other examples of actuation of the ****** circuit shown in drawing 37 .

[Drawing 40] It is a conceptual diagram of operation for explaining an example of further others of actuation of the ****** circuit shown in drawing 37 .

[Drawing 41] In order to explain other one example of ****** concerning this invention, and ****** actuation, it is a wave form chart.

[Drawing 42] It is bit pattern drawing showing one example of the non-corresponded number MK of drawing 41 .

[Drawing 43] It is the block diagram showing one example of the digital signal regenerative circuit to the digital signal with which the data compression was performed which already hears it and contains /****** mode.

[Drawing 44] It is the block diagram showing one example of the data-conversion circuit constituted by the data-conversion method concerning this invention.

[Drawing 45] It is a wave form chart for explaining an example of the analog / digital conversion actuation accompanied by data compression actuation of drawing 44 .

[Drawing 46] It is the block diagram showing other one example of the data-conversion circuit constituted by the data-conversion method concerning this invention.

[Drawing 47] It is the block diagram showing one example of the digital to analog circuit concerning this invention.

[Drawing 48] It is the wave form chart showing an example of actuation of the digital to analog circuit of drawing 47 .

[Drawing 49] It is the block diagram showing other one example of the digital to analog

circuit concerning this invention.

[Drawing 50] It is the block diagram showing one example of further others of the digital to analog circuit concerning this invention.

[Drawing 51] It is the fundamental block diagram showing one example of the switch input circuit of the player used for a digital signal delivery system.

[Drawing 52] It is the block which shows one example of the concrete configuration of an operating state control circuit.

[Drawing 53] It is a conceptual diagram for explaining the mode of operation of the example of drawing 52 .

[Drawing 54] It is the block which shows other one example of the concrete configuration of an operating state control circuit.

[Drawing 55] It is a conceptual diagram for explaining the mode of operation of the example of drawing 54 .

[Drawing 56] It is the block diagram showing one example of the storage region management method of the store circuit carried in a player.

[Drawing 57] It is the conceptual diagram of one example of the storage region management method of the store circuit built in a player.

[Drawing 58] It is the conceptual diagram of other one example of the storage region management method of the store circuit built in a player.

[Drawing 59] It is the important section block diagram showing one example of the player at the time of adding the table-of-contents function of drawing 58 .

[Drawing 60] It is the block configuration which shows one example of the same player as drawing 7 .

[Drawing 61] It is the block diagram showing one example in the case of widening a store circuit in the example of drawing 60 .

[Drawing 62] It is the important section block configuration which shows one example of a self-test circuit.

[Drawing 63] It is outline drawing of Type I of the memory card by JEIDA specification.

[Drawing 64] It is outline drawing of Type II of the memory card by JEIDA specification.

[Drawing 65] It is the table showing the pinout of the memory card by JEIDA specification.

[Drawing 66] It is the table showing the signal property of the memory card by JEIDA specification.

[Drawing 67] It is drawing showing the appearance of one concrete example of the digital signal delivery system concerning this invention.

[Drawing 68] It is drawing showing the appearance of other one concrete example of the digital signal delivery system concerning this invention.

[Drawing 69] It is drawing showing the appearance of one example with still more concrete others of the digital signal delivery system concerning this invention.

[Description of Notations]

100 -- A terminal unit, 101 -- A memory card with a regenerative function (player), 102 [-- VME bus,] -- The input section, 103 -- The storage section, 104 -- The output section, 105 201 -- The network interface corresponding to B-ISDN, 202a, 202b -- Low pass filter, 203 -- A multiplexer, 204 -- A sample hold circuit, 205 -- An analog / digital conversion circuit, 206 -- An input section control circuit, 207 -- Digital input interface, 301 -- A hard disk, 302 -- A hard disk control circuit, 303 -- Liquid crystal display, 304 -- A LCD control circuit, 305 -- A VME interface, 306 -- Microprocessor, 307 -- Read only memory (ROM), 308 -- Random access memory (RAM), 309 -- An internal bus, 401 -- An output interface, 402 -- A memory card control circuit with a regenerative function, 403 -- Buffer memory, 404 -- A monitor control circuit, 405 -- Monitor, 406 [-- Photosensor,] -- A loudspeaker, 407 -- A power circuit, 501 -- An input buffer, 502 503 -- I-V amplifier, 504 -- A serial/parallel-conversion circuit, 505 -- PLL oscillator circuit, 506 -- A frequency divider, 507 -- A multiplexer, 508 -- Mode switch, 601 -- An output buffer, 602 -- A parallel/serial-conversion circuit, 603 -- Start bit addition circuit, 604 -- V-I amplifier, 605 -- A laser diode, 701 -- Store circuit, 702 -- A multiplexer, 703 -- An address counter, 704 -- Control circuit, 705 -- A parallel/serial-conversion circuit, 706 -- Low pass filter, 707 -- A digital to analog circuit, 708 -- An amplifying circuit, 709 -- Large-scale integrated circuit (gate array), 710 -- A power circuit, 711 -- An earphone jack, 801a-801h -- 4Mb false [SRAM] (static random access memory) 802 -- A memory board, 803 -- A flexible wiring substrate, 804 -- Connector, 805 -- An amplifying-circuit component, 806 -- An amplifying-circuit component, 807 -- Control substrate, 808a-808d -- A carbon button cell, 1001 -- The store circuit section, 1002 -- Store circuit section connector, 1101 -- A control circuit, 1102 -- A store circuit, 1103 -- Store circuit section connector, 1104 -- A multiplexer, 1105 -- A multiplexer, 1106 -- Address counter, 1201 [-- Cell,] -- Diode, 1202 -- Diode, 1203 -- A cell, 1204 1205 [-- Bit 0 (D0),] -- A cell, 1206 -- A switch, 1207 -- A switch, 1300 1301 -- Bits 1 (D1) and 1302 -- Bits 2 (D2) and 1303 -- Bit 3 (D3), 1304 -- Bits 4 (D4) and 1305 -- Bits 5 (D5) and 1306 -- Bit 6 (D6), 1307 -- Bits 7 (D7) and 1308 -- An ID code, 1309 -- Data, 1401 -- A register, 1402 -- An oscillator circuit, 1403 -- Clock pulse generating circuit, 1404 -- A multiplexer, 1405 -- A bit length conversion circuit, 1500 -- Quantizing-noise clearance circuit, 1501 -- A comparator, 1502 -- An AND circuit, 1503 -- Counter, 1504 -- A comparator, 1505 -- A logical negation circuit, 1507 -- Level judging circuit, 1508 -- A timer circuit, 1509 -- A comparator, 1510, 1511-151n -- AND circuit, 1600a -- The signal before processing, 1600b -- The signal after processing, 1700, 1701-170n -- Exclusive "or" circuit, 1800, 1801-180n -- An exclusive "or" circuit, 1900, 1901-190m -- Exclusive "or" circuit, 2000-200n -- An exclusive "or" circuit, 2010-201n -- Exclusive "or" circuit, 2101 -- A rearrangement circuit, 2201 -- A change-over circuit, 2202 -- Decoder, 2203 -- A multiplexer, 2204 -- A random-number circuit, 23000, 23001-2300n -- Buffer circuit,

2301 -- An AND circuit, 2302 -- A logical negation circuit, 24000, 24001-2400n -- Buffer circuit, 24010, 24011-2401n -- An AND circuit, 2402 -- Logical negation circuit, 25000-2500m -- An AND circuit, 2501 -- A logical negation circuit, 2801 -- Rearrangement circuit, 2901 -- A change-over circuit, 2902 -- A decoder, 2903 -- Multiplexer, 2904 -- A random-number circuit, 3001 -- Headphone, 3002 -- Silent period detector, 3003 -- It is already heard and is a /****** circuit and 3101. -- A multiplexer, 3102 -- Logical negation circuit, 3103 -- An AND circuit, 3201 -- A flip-flop circuit, 3202 -- Silent period counter, 3203 -- A comparator, 3204 -- N counter, 3205 -- Counter, 3206 -- An AND circuit, 3207 -- A logical negation circuit, 3208 -- AND circuit, 3209 -- A logical negation circuit, 3210 -- An AND circuit, 3211 -- AND circuit, 3301 [-- Silent period,] -- The HARASHIN number, 3302 -- A processing signal, 3303 -- A silent period, 3304 3401 [-- Adder circuit,] -- A processing signal, 3402 -- A silent period, 3403 -- A silent period, 3501 3502 -- A register, 3503 -- An address counter, 3504 -- Multiplexer, 3505 -- An AND circuit, 3506 -- A logical negation circuit, 3601 -- Multiplexer, 3602 -- An AND circuit, 3603 -- A logical negation circuit, 3701 -- OR circuit, 3702 -- The counter for extension, 3703 -- A multiplication circuit, 3704 -- Comparator, 3705 -- A multiplexer, 3706 -- A comparator, 3707 -- Comparator, 3708 -- An AND circuit, 3709 -- A logical negation circuit, 3710 -- AND circuit, 3711 -- An AND circuit, 3712 -- An AND circuit, 3713 -- Logical negation circuit, 3714 -- A flip-flop circuit, 3801 -- The signal before processing, 3802 -- The signal after processing, 3901 -- The signal before processing, 3902 -- The signal after processing, 4001 -- The signal before processing, 4002 [-- A silent mark, 4204 / -- Silent period information, 4301a-4301d / -- A shift register, 430] -- The signal after processing, 4101 -- A processing signal, 4102 -- The maximum of a silent signal and a 4201--8-bit two's complement code, the minimum value of a 4202--8-bit two's complement code, 4203 2a-4302d -- A D-type-flip-flop circuit, 4303 -- Mark detection circuit, 4304 -- A comparator, 4305 -- A silent counter, 4306 -- Repeat counter, 4307 -- 4308 A comparator, 4309 -- Flip-flop circuit, 4310-4312 -- 4313 An AND circuit, 4314 -- Logical negation circuit, 4315 -- An OR circuit, 4401 -- An analog / digital conversion circuit, 4402 -- A subtractor circuit, 4403 -- A comparator, 4404 -- Selector, 4405 -- An adder circuit, 4406 -- A register, 4407 -- Criteria data, 4408 -- A store circuit, 4501 -- An analog signal, 4502 -- The digital signal after compression, 4601 [-- Digital to analog circuit,] -- A store circuit, 4602 -- An adder circuit, 4603 -- A register, 4604 4701 -- A register, 4702 -- A comparator, 4703 -- Counter, 4704 -- A repeat counter, 4705 -- A control circuit, 4706 -- Resistance, 4707 -- A capacitor, 4708 -- A low pass filter, 4901 -- Down counter, 4902 -- A flip-flop circuit, 4903 -- Resistance, 4904 -- Capacitor, 4905 -- A low pass filter, 5001 -- A down counter, 5002 -- Rise counter, 5003 -- A flip-flop circuit, 5004 -- A control circuit, 5005 -- Logical negation circuit, 5006 -- An AND circuit, 5007 -- A low pass filter, 5101 -- Switch, 5102 -- An operating state control

circuit, 5103-1 - 5103-n -- Operating state 1-n, 5201-1 -- Condition A, 5201-2 -- Condition B, 5201-3 -- Condition C 5301a [-- Condition A] -- Condition A, 5301b -- Condition A, 5301c -- Condition B, 5301d 5301e [-- Time amount referee conditions,] -- Condition C, 5302 -- A idle state, 5303 -- A playback condition, 5304 5305 -- A halt condition, 5401-1 -- Condition A, 5401-2 -- Condition B 5501a [-- Condition B] -- Condition A, 5501b -- Condition A, 5501c -- Condition A, 5501d 5501e -- Condition B, 5601 -- A block-address store circuit, 5602 -- The address counter for block addresses, 5603 -- A decoder circuit, 5604 -- An indicator, 5605 -- Chatter killer circuit, 5606 -- An OR circuit, 5607 -- A switch, 5608 -- Delay circuit, 5609 -- An OR circuit, 5610 -- A data store circuit, 5611 -- The address counter for data, 5612 -- Logical negation circuit, 5701a [-- ID codes 1 and 5702a / -- Tables of contents 2 and 5702d / -- Data 2 and 5702e / -- End marks 2 and 5702i / -- ID codes 2 and 5703a / -- Tables of contents 3 and 5703d / -- Data 3,] -- Tables of contents 1 and 5701d -- Data 1 and 5701e -- End marks 1 and 5701i 5703e [-- Data 4 and 5704e / -- End marks 4 and 5704i / -- ID codes 4 and 5801 / -- Table-of-contents store circuit,] -- End marks 3 and 5703i -- ID codes 3 and 5704a -- Tables of contents 4 and 5704d 5802 -- A data store circuit, 5901 -- A table-of-contents address counter, 5902 -- Data-address counter, 5903 -- A register, 5904 -- A register, 5905 -- Comparator, 5906 [-- Table-of-contents register,] -- A control circuit, 5907 -- A switch, 5908 -- A switch, 5909 5910 -- A liquid crystal display, 6001 -- 1 chip integrated circuit, 6101 -- Extended address counter, 6102 -- An extended multiplexer, 6103 -- An address escape circuit, 6104 -- Extended store circuit, 6201 -- A counter, 6202 -- A multiplexer, 6203 -- Comparator, 6204 -- A buffer circuit, 6205 -- A negative OR circuit, 6206 -- Delay circuit, 6207 -- First in first out memory, 6210 -- AND circuit, 6211 [-- An OR circuit, 6215 / -- An OR circuit, 6216 / -- A logical negation circuit, 6701 / -- Player insertion opening, 6701 / -- An actuation switch group, 6901 / -- Check switch.] -- An AND circuit, 6212 -- An AND circuit, 6213 -- An OR circuit, 6214